The DARE Library family

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ESA/ESTEC Noordwijk – NL

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In a nutshell...

• The DARE library family supports design of ASICS for spacecraft
  – Uses commercially available technology without change
  – Using the library is free of charge for European space industry
  – Customer can do front-end design (to netlist)

• Physical implementation services provided by imec
• Manufacturing, Packaging, qualification & Radiation test up to FM is supported

• Flexible solution
  – DARE allows for mixed signal design
    • Can add specific analog blocks; designed by you, a design house or imec
  – Cells can be added to the library
The DARE180 standard cell library family

- Developed in several ESA projects
- DARE = Design Against Radiation Effects (=RHbD)
- Commercial Technology: UMC L180 CMOS

- TID hardness is far beyond requirement level for geostationary orbit
  - Tested to 1 MRad
- No SEL, SEFI, SEH seen so far
- Low SEU sensitivity, compatible with geostationary orbit mission
  - ‘normal’ flip-flops & RAMs
  - HIT-based flip-flops are very insensitive to SEU
    - New test data from 2 designs will come available later this year
## Libraries

<table>
<thead>
<tr>
<th>IO at 3.3 and 2.5 V</th>
<th>Logic</th>
<th>CIS</th>
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<tbody>
<tr>
<td>Core 1.8V</td>
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<tr>
<td>combinatorial</td>
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<tr>
<td>normal' FF's</td>
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<td>20</td>
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<td>HIT FF's</td>
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<tr>
<td>Digital IO 110x110</td>
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<tr>
<td>IO</td>
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<td>Analog IO 110x110</td>
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<tr>
<td>IO</td>
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<tr>
<td>LVDS 70x70</td>
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<tr>
<td>LVDS 110x110</td>
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<tr>
<td>IO</td>
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<tr>
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<tr>
<td>PLL 110x110</td>
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<td>1</td>
</tr>
<tr>
<td>SRAM Compiler (6Tor cell)</td>
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</table>

All FF’s have scan equivalents

+ fillers & Corners

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DARE vs a commercial .18 library

- Maximum gate density = 25Kgates/mm²
- DARE cells are 2 - 4 times bigger than cells with same functionality from a commercial library
- DARE vs commercial cell power = 2.2x
  - Total power = Internal & Switching power
- No speed penalty
- Views available for a classical ASIC design flow
  - Using the HIT flip-flops no triplication is necessary
- Designs with a lot of RAM become very big
- SEU Hardening of RAM using EDAC circuit
How to get access

• Get in touch with Steven.Redant@imec.be
  – By mail, or by asking access to the library files on the web

• Sign NDA (per project)

• Get access to the download area on the web
  – www.europractice-online -> UMC -> Radiation-Tolerant-Library

• Download the (Front End) views
  – Synthesis & Simulation
One interface, including customer support

- Detailed Requirements Specification
- Front-End Design
- VHDL, Constraints
- Back-End Design
- ASIC Layout (GDSII)
- Digital Design Kit
- Digital Library Design
- Analogue Design Kit
- IMEC
- Foundry
- Evaluation
- Assembly
- Wafers
- Components
What is behind it...

- Detailed Requirements Specification
- Front-End Design
- Back-End Design
- VHDL, Schematics, Constraints
- Digital Design Kit
- Digital Library Design
- Analogue Design Kit
- ASIC Layout (GDSII)
- UMC
- IMEC

Evaluation
- Microtest, MAPRAD, Maser
- Test House

Assembly
- e.g. HCM
- Assembly House
- Wafers

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imec contact persons

**INVOMEC**

- **H. Maes**

**ASIC Services**
- **Carl Das**

**EUROPRACTECE**

**Design Services**
- **Steven Redant**

**First contact:**

- **Library Development & Design Services**
  - **Team SVP**
    - **Danny Lambrichts**
    - **Paul Malisse**
    - **Luc Laeveren**
    - **AMS, MEMS**
    - **Carl Das**

- **Team DSBE**
  - **Luc Folens**
  - **Geert Vanwijnsberghe**

- **Team DSFCL**
  - **Geert Thys**

**Manufacturing, Packaging & Testing Services**

- **Team UMC**
  - **Tapeout & Manufacturing follow-up**
  - **Paul Malisse**

- **Team TSMC**
  - **Luc Laeveren**

- **Team OnSemi,AMS,MEMS**
  - **Carl Das**

- **Team DSFE**
  - **P&R**
  - **front-end Services (if needed)**
  - **Geert Vanwijnsberghe**

- **Team DSBE**
  - **Luc Folens**

- **Team DSFCL**
  - **Geert Thys**

- **DARE development and support Analog design (if needed)**
 Backend services

- IMEC has been running a backend service for 12 years now
  - Excellent first-time-right record
  - >13 foundries have been covered
  - Knowledge of Low power methods

- Customer delivers netlist (or VHDL) & constraints (or documentation)

- IMEC
  - (synthesis)
  - P&R (incl. tapeout checks)
  - provides backannotation information to customer
  - Additional design services can be discussed about
    - E.g. if an analog block is needed

- Customer gives tapeout ok!
MPW’s & full mask sets

- **(Europractice) MPW’s**
  - Scheduled UMC runs (pure logic runs are limited)
  - Apply for MPW slot >1 month in advance
  - 50 samples
  - .18: ±14k EUR/ 5x5mm square
  - Extra wafer (± 1900 EUR) => 30 extra dies per wafer
  - = Prototyping to prove functionality
    - Dies from WAT accepted wafers
    - No wafers delivered!

- **Single project Wafer runs**
  - Full Mask set => More expensive
  - Can start any time
  - More possibilities w.r.t. probing, holding at metal, wafer delivery, quality documentation, ...
  - Necessary for QM & FM in space projects.
Packaging & FM Qualification

- Package choice support
  - Packageability
  - Radiation testability
  - Qualifiability
  - Availability

- Full qualification flow set up with subcontractors
- Space qualification according to ESCC9000
  - Assembly of the ASIC, Chart F2
  - Screening of the ASIC, Chart F3
  - Qualification of the ASIC, Chart F4

- Radiation tests
Legacy is building up

- Delivery of first DARE180 based FM’s mid 2010
- Tapeout of imager prototype project imminent
- Talking to several new interested parties
Future

- **Additions to DARE180**
  - Fix a known problem in the RAM compiler
  - FP7 project submitted to
    - standardize flow for digital circuits
    - Add a High Speed Serial Link
  - Other possibilities (activity is in the pipeline)
    - DPRAM, 2PRAM, FIFO
    - RF tech characterization
    - Core cells @ 3.3V (=> I/O and core at same voltage)
    - Clock gating cells
    - 5V tolerant I/O, Cold Sparing I/O, ...
    - ...
  - DARE is a flexible solution

- **DARE90**
  - 90 nm test vehicle
    - TID test done (up to 2 MRad, 90nm is quite hard in itself)
    - SEE test to be done
  - Library definition & Start of implementation: later in 2010
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