Exoplanet Characterisation Observatory (EChO)

Assessment Phase Payload Study

EChO electronics

ECHO-TN-0003-INAF

Issue 1.1

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1.0	‘13/9/15	All	Baseline detectors selection has changed	First release
1.1	‘13/12/02	All	Changed numeration	v. 1.1

DISTRIBUTION LIST

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	T Guillot				
	Others…				

TABLE OF CONTENTS

1 PREAMBLE

1.1 SCOPE

This document covers the EChO Payloads electronics aspects. It is a TN report on the overall electronics subsystems characterising the present instrument configuration in order to give an overview of the Payload's electrical and electronics architecture and a basic definition for the analog and digital data paths from the scientific modules/channels detectors to the Instrument Control Unit (ICU), as unique scientific data interface hosting on-board data processing resources to the spacecraft.

1.2 PURPOSE

The purpose of this document is to provide an updated overview on the EChO Payloads electronics at the end of the Assessment Study (Phase A), with particular regards to the Instrument Control Unit (ICU), its own electrical, mechanical and thermal interfaces and data processing resources.

1.3 APPLICABLE DOCUMENTS

AD #	APPLICABLE DOCUMENT TITLE	DOCUMENT ID	ISSUE / DATE
1	EChO EID-A	ECHO-SRE-F/2012.097	V0.2 / 22-4-13
2	EChO Environmental Specification	JS-1-12	V1 / 12-1-12
3	EChO Mission Requirements Document	SRE-PA/2011.038	V3 / 12-9-12
4	EChO Scientific Requirements Document	SRE-PA/2011.037	V3 / 14-9-12
5			

1.4 REFERENCE DOCUMENTS

RD #	REFERENCE DOCUMENT TITLE	DOCUMENT ID	ISSUE / DATE
1	EChO EID-B	ECHO-RS-0002-RAL	V0.1 / 30-11-12
2	EChO DCU Simulator description	ECHO-IAA-SP-0001	V1 / 10-09-12
3			

2 INTRODUCTION

The Exoplanet Characterisation Observatory (EChO) is one of the candidates of the ESA Cosmic Vision M3 medium-class mission competition. It aims at the characterisation of the atmospheres of a selected targets sample of recently discovered transiting extra-solar planets. The EChO payload is a fully integrated remote-sensing spectrometer based on a dispersive spectrograph covering continuously the 0.55-11 μm (0.4–16 μm as a goal) spectral range. It is subdivided into 4+1 main modules from visible to thermal IR (VNIR, SWIR, MWIR -2 channels-, LWIR, FGS- Fine Guidance System) with different spectral resolutions and a common set of optics spectrally dividing the field of view by means of dichroics and a beam splitter.

The aim of the integrated spectrometer is to perform time-resolved spectrophotometry exploiting the temporal and spectral variations of the signal due to the primary and secondary occultations occurring between the exoplanet and its parent star in order to extract the planet spectral signature and probe the physical and chemical properties of its atmosphere.

The instrument will be mounted behind a passively cooled 1.2 m class telescope and a common set of optics and dichroics able to spectrally split the atmospheric signatures from the visible light to the mid-infrared range feeding 4 different scientific detectors based on MCT (Mercury-Cadmium-Telluride) and Si:As, as baseline, for the longest wave channel.

The present TN is written to provide an overview of the electrical and electronics adopted architecture as a baseline result of the trade-off processes between system budgets (ref. EChO EID-A) and the overall system complexity as driven by the scientific requirements and mission requirements (ref. EChO SciRD and MRD).

3 ECHO PAYLOAD ELECTRICAL ARCHITECTURE

The EChO payload overall electrical architecture (Figure 1, 2 and 3) can be basically subdivided in two sections: spectrometer's FPA detectors with their ROICs (Read Out Integrated Circuits) and cold front-end electronics (CFEEs) on one side and warm electronics on the other side. The cold detectors cavities are maintained @ ~45 K in order to meet the strict operative thermal requirements and are connected to the CFEEs and to the warm electronics by means of very low thermal conductance cryo-harnessing.

With reference to Figure 1 and 2, the FPAs analog readout signals are locally amplified by the ROICs and converted to digital values inside the A/D Cold front End Electronics (CFEEs) represented by ASICs (Application Specific Integrated Circuit) devices.
The currently adopted ICU architecture interfaces the SIDECAR ASICs from Teledyne by means of WFEEs, one per each scientific focal plane array (spectrometer), which shall be connected to the CFEEs and detectors modules by means of suitable cryo-harnessing.
The digital signals are then handled by the warm front end electronics (WFEEs), which are located at a ~2.5÷3 m distance from FPA, and sent to ICU (Instrument Control Unit). The ICU will provide the main functionalities to manage all the instrument subsystems implementing detectors commanding, science and housekeepings (HKs) data acquisition and A/D conversion, calibration sources and mechanisms (if occurring) management and the overall on-board communication management.

In principle it may be possible to interface the ICU directly to the SIDECAR ASICs, as reported in Figure 3, negating the need for the WFEEs. This architectural change will be studied in more detail in the next phase and finalised before the SRR.

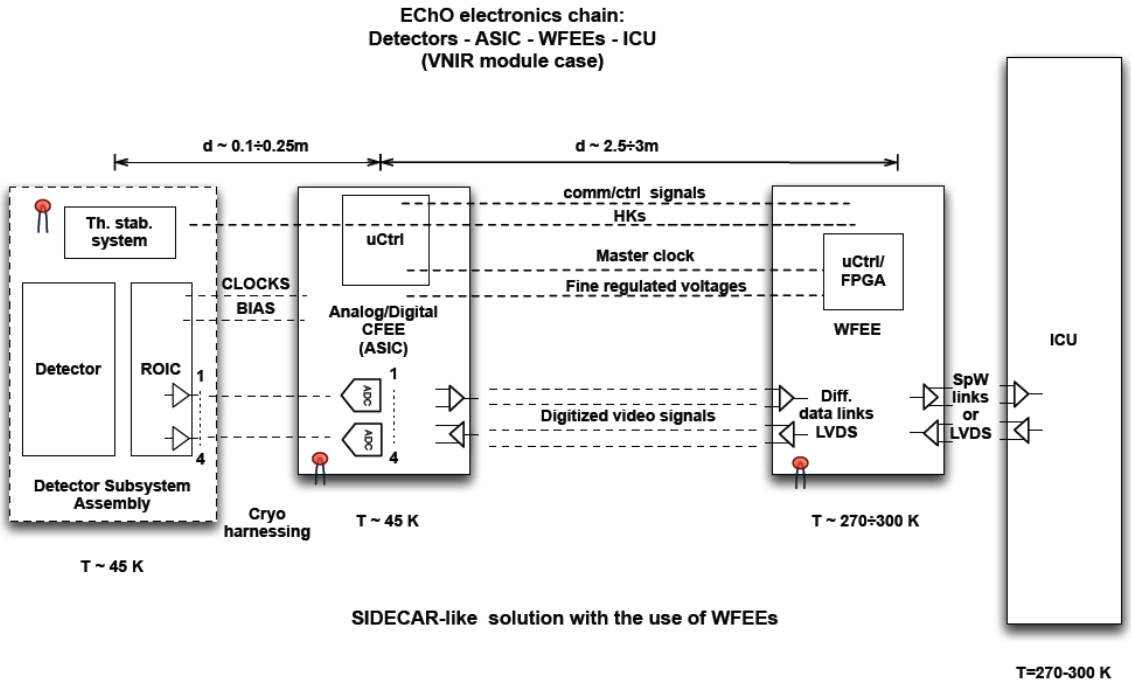

Fig. 1 - EChO payload overall electrical architecture (baseline solution with SIDECAR ASIC and WFEE).

ICU will implement the unique payload instruments interface to the S/C Data Management System (OBC+SSMM) hosting nominal and redundant connections for telemetry (TM), telecommand (TC), housekeeping and power supply lines.

ICU and WFEEs, being warm electronics units operating at ~273-300 K, will be located inside the SVM (Service Vehicle Module), a module thermally decupled by the telescope optical bench.

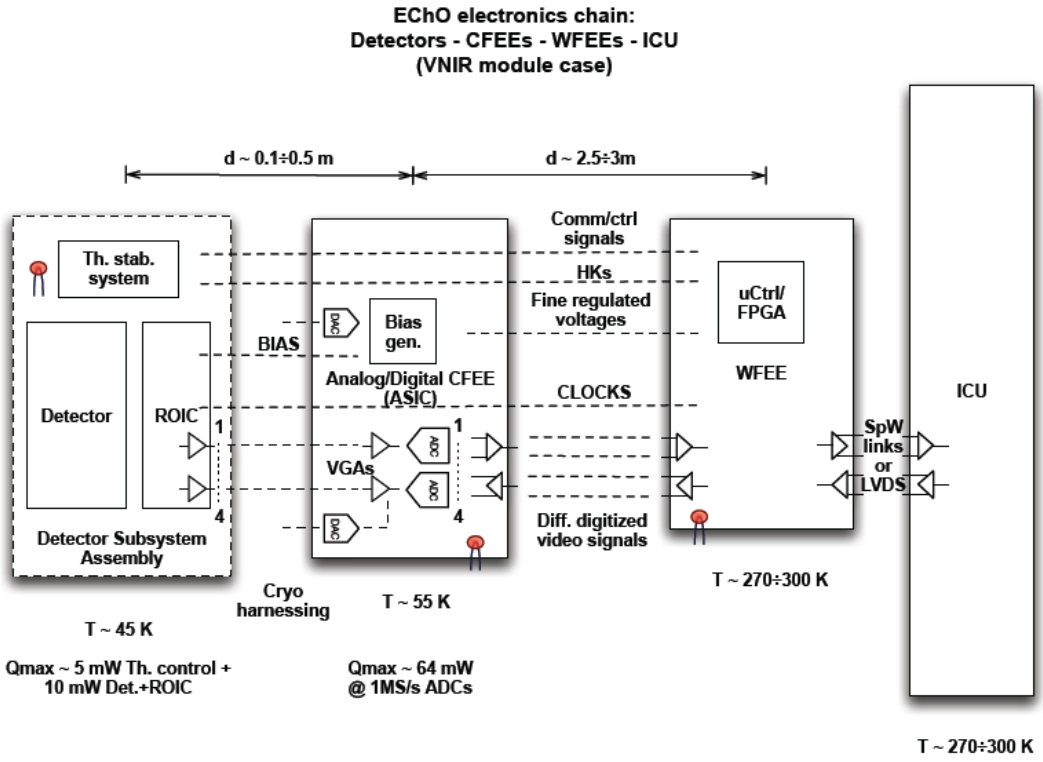

Fig. 2 - EChO payload overall electrical architecture (alternative solution with SRON ASIC and WFEE).

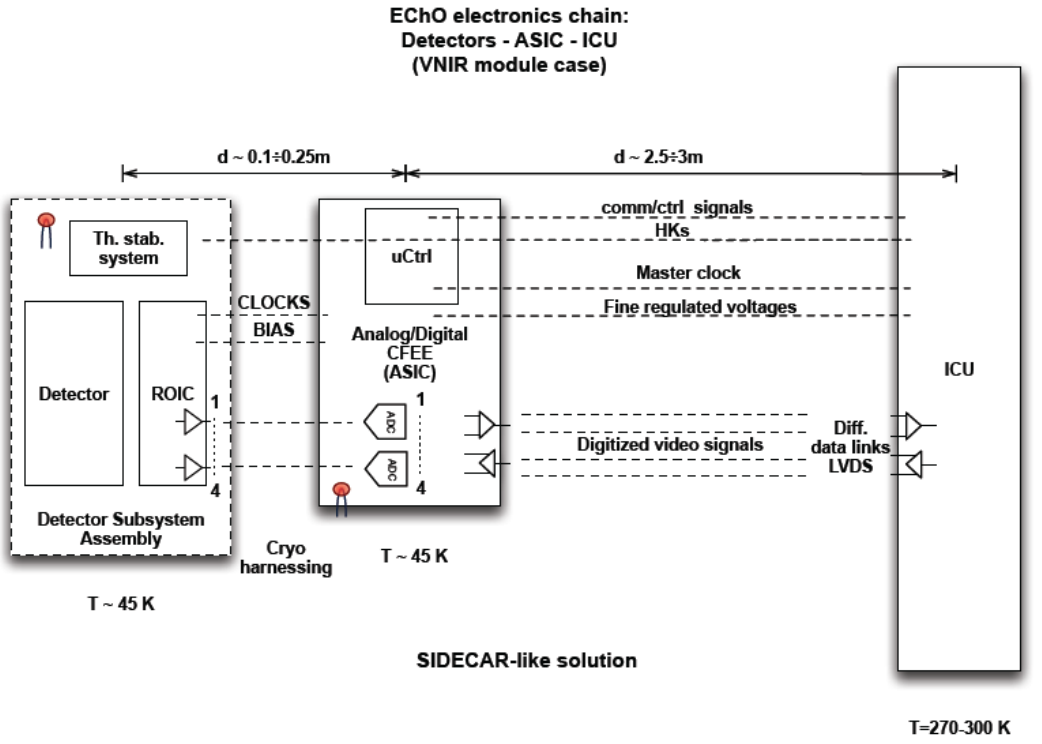

Fig. 3 - EChO payload overall electrical architecture (a possible solution without adopting WFEEs and interfacing directly the SIDECAR ASIC to the ICU).

ICU is structured in three main sub-units:

1. *Data Processing Unit (DPU)*: a digital sub-unit with processing capabilities. Its architecture is based on a rad-hard space qualified processor running the main Application SW (data processing SW) and some digital logics (two FPGA as baseline). The DPU will implement the scientific digital data on-board processing, the data storage and packetisation, the telemetry and telecommand packets handling and the clock/synchronization capability to temporally correlate the scientific data coming from the different spectrometer channels.
2. *Housekeeping and Calibration source Unit (HCU)*: a sub-unit designed to provide instrument/channel thermal control, calibration source and HKs management with the aim of a second rad-hard space qualified processor running the main Application SW (instrument control SW), as baseline, and an FPGA.
3. *Power Supply Unit (PSU)*: it will distribute the secondary voltages to the instrument subsystems and ICU boards by means of DC/DC converters.

A single common TM/TC interface is foreseen at ICU level to minimize and simplify the number of interfaces towards the spacecraft. The ICU electronics will rely on a cold-strapped redundant architecture with some trade-off solutions removing or reducing any electronics single-point failure.

3.1 DETECTORS

3.1.1 Baseline adopted solution

In the baseline payload design all spectrometer modules will host MCT-type detectors (Figure 4) from Teledyne (for the LWIR channel are evaluated, as a possible choice, Si:As-type detectors) electrically and mechanically bonded with their ROICs. All ROICs will have at least four or more analog outputs, amplified and interfaced with their own CFEE (the SIDECAR ASIC), maintained at a temperature of ~45÷50 K, where analog to digital conversion will take place (SIDECAR can run with up to 36 ADC with a maximum sampling frequency of 500 KHz). The detectors for the VNIR, SWIR and FGS modules will be MCT (HgCdTe) arrays with 18 μm pixel pitch from Teledyne.
The detectors FPAs + CFEEs overall power dissipation allocation shall be a function of wavelength in order to limit the total thermal load from cold module to < TBD mW (about 80 mW are allocated for the VNIR cold electronics, see ECHO-TN-0001-IASFBO for more thermo-mechanical details). This value will include dissipation from the single detector and its thermal stabilization electronics, CFEE, parasitic loads (conductive and radiative) and all other loads caused directly by the cold-part module.

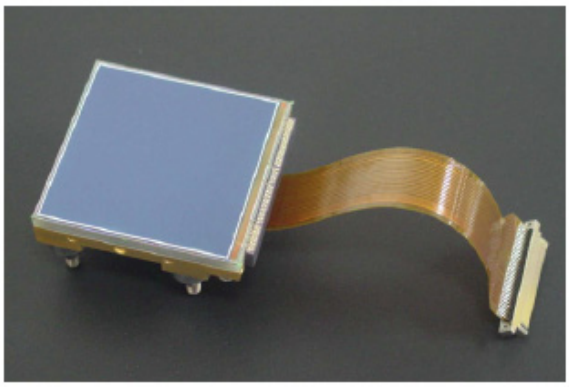

Fig. 4 – Example of a MCT detector from Teledyne. A 2k x 2k H2RG hybrid array characterised by a 18 μm pixel pitch.

3.1.2 Alternative solution

As a possible alternative solution we adopt for the VNIR, SWIR and FGS modules the MCT European detectors from Selex (arrays of 512 x 512 pixels with 15 µm pixel pitch) and an ASIC for CFEEs from the Dutch SRON.

3.2 COLD FRONT END ELECTRONICS (CFEES)

3.2.1 Baseline adopted solution

The foreseen baseline solution adopts SIDECAR ASIC from Teledyne as CFEEs for the VNIR, SWIR, MWIR and FGS modules (see Figure 5, 6 and 7 and Tables 1 and 2 for the ASIC's main characteristics). The present solution is the best one to drive properly the MCT detectors and to save mass, volume and power at the same time.

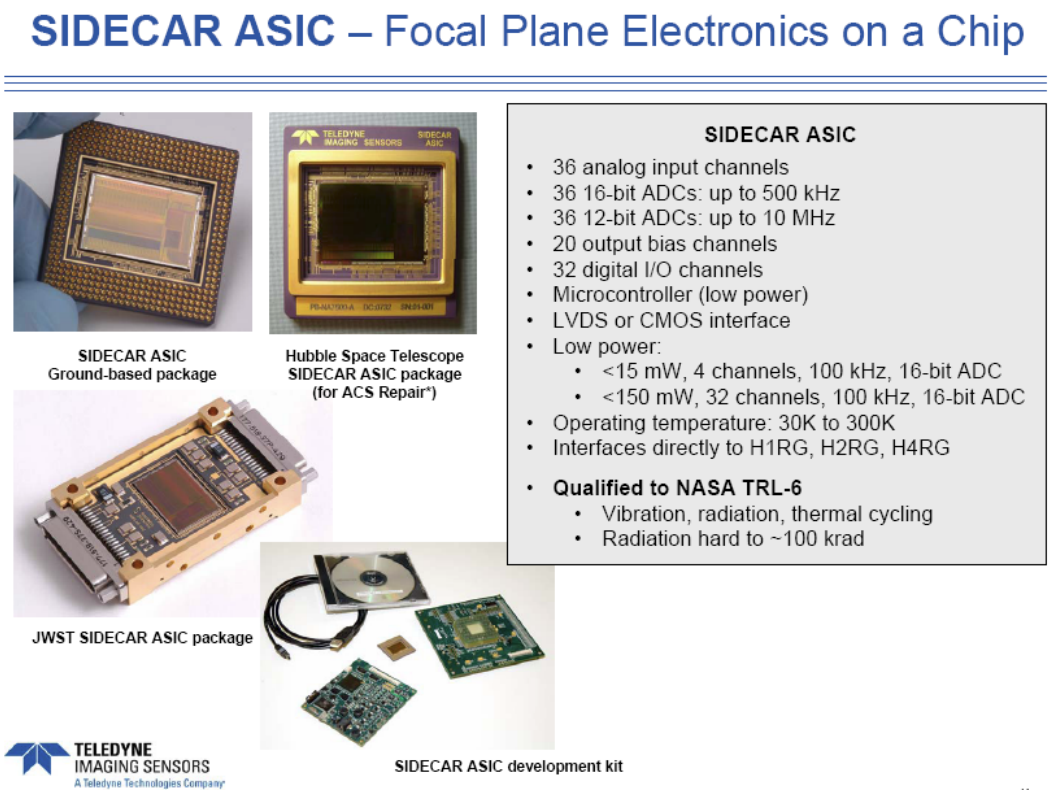

Fig. 5 – SIDECAR ASIC from Teledyne.

To greatly improve Sensor Chip Arrays (SCAs) integration by reducing size, overall system performance, Teledyne has developed the SIDECAR (System for Image Digitization, Enhancement, Control And Retrieval) ASIC. SIDECAR is a SCA interface chip that provides clocks and biases to the SCA, and performs amplification and analog-to-digital conversion of the SCA analog outputs. SIDECAR has 36 analog input channels, and digitization can be done with 12 or 16 bit resolution. SIDECAR presents all-digital interface to the external world, providing the following advantages to system design:

- Simplifies the overall system architecture and reduces the number of wires within the system;
- Eliminates the risks and problems of transmitting low-noise analog signals over long distances;
- Offers high flexibility and redundancy due to broad programmability;
- Digitises 16-bit data at 500 kHz (per port) or 12-bit data at up to 10 MHz (per port) for a maximum total of 12-bit pixel rate @ 160 MHz.

Figure 6 shows a schematic electrical diagram of the SIDECAR ASIC and its interfaces with the detector (i.e. ROIC multiplexer) and the host (external) electronics.

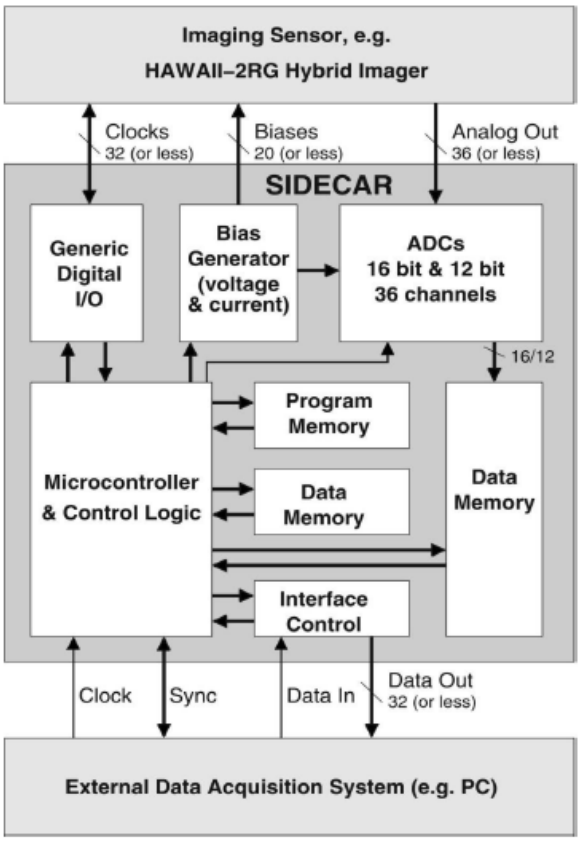

Fig. 6 – SIDECAR electronics block diagram.

Die Dimension	22 x 14.5 mm²
Technology	0.25 µm CMOS
Analog Input	36 independent channels, fully differential
Preamplifiers	Programmable gain (-3 to 27 dB) and bandwidth
16 bit ADCs	Up to 500 kHz sample rate (1 mW / channel at 100 kHz)
12 bit ADCs	Up to 10 MHz sample rate (10 mW / channel at 5 MHz)
Bias Outputs	20 output channels, selectable voltage or current DACs
Digital I/O	24 channels (CMOS), 16 channels (LVDS) fully programmable
Micro-controller	16 bit RISC, low power, excellent arithmetic capabilities
Program Memory	16 kwords (16 bit / word)
Data Memory (µC)	8 kwords (16 bit / word)
Data Memory (ADC)	36 kwords (24 bit / word)
Array-processor	Adding & multiplying and DMA control per ADC channel
Digital Interface	LVDS or CMOS, custom serial protocol, up to 32 parallel lines
Operating Temperature range	30 K – 300 K
Radiation	Complete design is single event upset protected

Tab. 1 – Summary of SIDECAR ASIC characteristics.

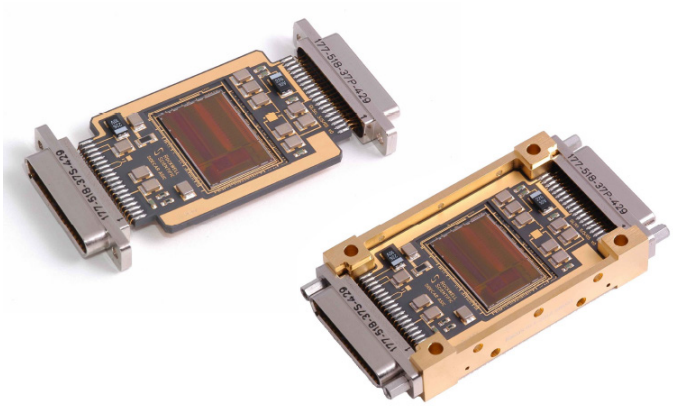

Fig. 7 – JWST flight package: ceramic circuit board with ASIC die and passive components, shown without and with metal housing. The dimensions are about 74 x 38 x 10.4 mm^3.

Component	Power Consumption
HAWAII-2RG	0.4 mW
16-bit ADCs (4 channels)	5.2 mW (1.3 mW / channel)
Preamplifiers (4 channels)	1.0 mW (0.25 mW / channel)
Bias generator	1.2 mW
Micro-controller & Clocking	1.5 mW
LVDS Driver	0.1 mW
Total Power	**9.4 mW**

Tab. 2 – Power consumption for the FPA operation with 4 channels including a H2RG detector.

3.2.2 Alternative solution

The CFEEs alternative solution adopts the SRON CFEE ASIC (Figure 8). It host up to 4 A/D converters @ 16 bits outputs with input VGA (Variable Gain Amplifiers) able to perform offset and gain corrections on the video input signal and at least an externally DAC-controlled fine bias generator, as baseline, to feed the detectors ROICs. A/D converters outputs are differentially interfaced to WFEEs in order to remove the common mode residual noise.

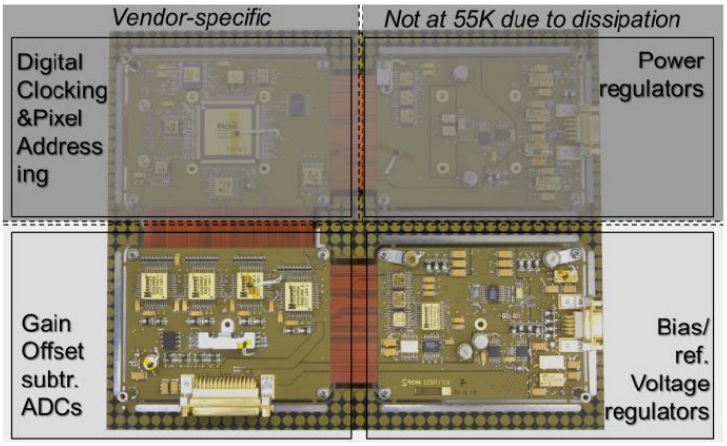

Fig. 8 - Functions implemented in the SRON ASIC are Gain offset subtraction and A/D conversion as well as bias and voltage regulation. Clocking, addressing and power regulation will not be done by this unit but inside the WFEE FPGA (courtesy SRON).

In order to prevent from and minimising all the likely conductive thermal leakages between the detectors and the CFEEs stages operating @ a delta-T of about 10÷15K, the FPAs and the CFEEs shall be electrically connected by harnessing ranging from few cm to about 50 cm (TBC). The increasing distance between units could represent a potential issue for pixels clocking and video signal driving from the detectors outputs to the CFEEs, requiring (TBC) an intermediate current buffering stage between the two units, especially when operating the detector at high readout frequencies. This solution would also increment the overall module electrical and electronics complexity leading to a revised basic solution adopting more than two outputs to operate the detectors (especially the VNIR channel one) in a low speed mode (below 500 kpx/s @ 16 bits/px) to limit power consumption/dissipation and electrical noise. The final adopted solution with the SRON ASIC should be a compromise between available budgets and the chosen sampling frequency to meet the scientific requirements.

3.3 WARM FRONT END ELECTRONICS (WFEES)

3.3.1 Baseline adopted solution

WFEEs (see Figure 9 and 10) are equipped with digital LVDS transceivers to communicate with CFEEs (to send/receive digital commands and collect digitised data) and host a digital logic (mainly an FPGA and/or a microcontroller, TBC) to produce command and control signals and digital clocks to manage the detectors ROICs and CFEEs (mainly the Master Clock and Sync signals for the SIDECAR ASIC).
In the baseline design the A/D conversion will be performed on board the CFEEs ASIC as well as detector clocking, wave shaping and filtering while spectra pre-processing (e.g. digital masking and image cropping - TBC) on board the WFEEs by means of a suitable FPGA, as reported in Figure 9.

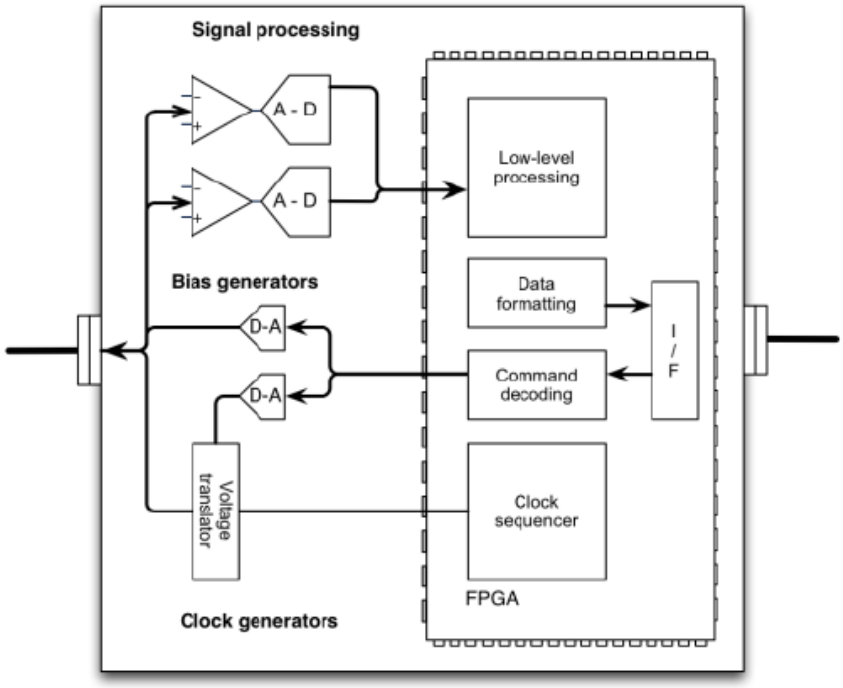

Fig. 9 – WFEEs electronics.

WFEEs also generate precise secondary voltage levels to feed the CFEEs electronics, which, in turn, produce fine-regulated biases for the detectors FPA assemblies.
WFEEs will be connected to the ICU by means of a nominal + a redundant SpW link or a LVDS I/F (TBD/TBC). These interfaces will be implemented by means of IP cores inside the hosted FPGA. A possible accommodation for the WFEE electronics boards (FGS excluded) is represented in Figure 10. The aluminium alloy box dimensions are 224x164x80 mm^3.

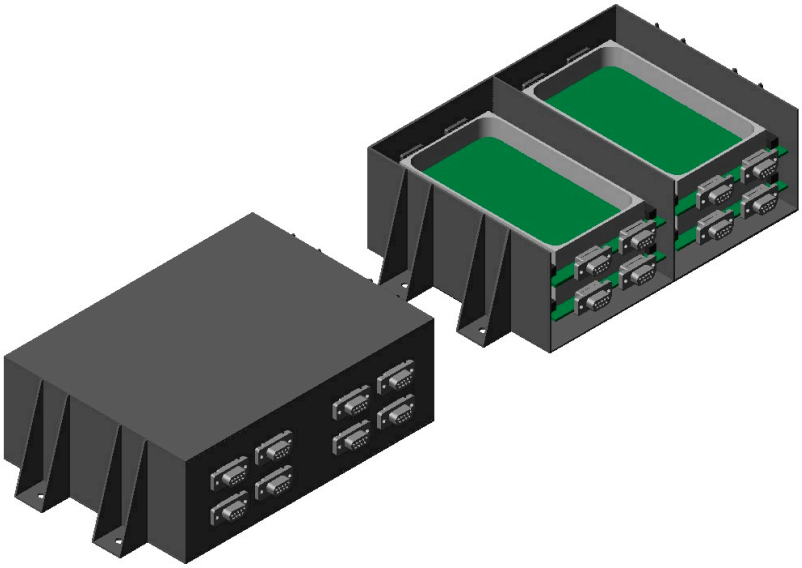

Fig. 10 – WFEEs mechanical design.

(connectors # and location are TBD/TBC and for illustration purpose only)

The WFEEs box mass and volume budgets (for 4 WFEEs) are reported in Table 3 with an estimate of the power consumption (TBC). The provided overall dimensions are not taking into account the box mounting feet.

Description	Basic (EID-A R-1880)	Nominal (with 20% contingency) (EID-A R-1890)	Margin (EID-A R-1910) (EID-A R-0570)
Power	< 18 W	< 21.6 W	< 2.4 W
Mass	3.5 kg	4.2 kg	Tot. electr. < 25 kg
Volume	224 x 164 x 80 mm^3	-	26 x 76 x 100 mm^3

Tab. 3 – WFEEs budgets.

3.3.2 Alternative solution

As a possible alternative solution (see Figure 3) we could interface directly the SIDECAR ASIC to the ICU, so no WFEEs are foreseen in that case.

3.4 FINE GUIDANCE SYSTEM (FGS)

For the FGS module we refer directly to "*FGS Electronics*", ECHO-TN-0001-UVIE, Issue 0.1 redacted by the Austrian and Polish teams.

4 INSTRUMENT CONTROL UNIT (ICU)

The EChO payload electrical architecture is designed to simplify the interfaces between the integrated spectrometer and the spacecraft and to suitably perform the required on-board scientific-data digital processing and instrument management.
As described in section 3, a single Instrument Control Unit is foreseen, implementing all payload instruments control functions and all detectors digital signals acquisition and processing.

4.1 ICU DESCRIPTION

The EChO payload electrical block diagram, as reported in Figure 11, focuses mainly on data and command flows, clock/synchronization and power distribution, data processing and data formatting. The cold proximity electronics are interfaced to the detectors ROICs bonded to the MCT sensors arrays in the VNIR, SWIR, MWIR and LWIR modules (the latter hosts a Si:As detector as baseline). These proximities will provide the amplified analogue HKs (temperatures, voltages and currents) to the warm front-end electronics and ICU, where multiplexing and HKs analogue to digital conversion will take place.
The proposed payload architecture has been designed to minimize and simplify the number of interfaces. In particular, the ICU will be the unique payload interface with the spacecraft Power Conditioning and Distribution Unit (PCDU) and the On-Board Computer (OBC) and Solid State Mass Memory (SSMM) – (ref. EChO EID-A).

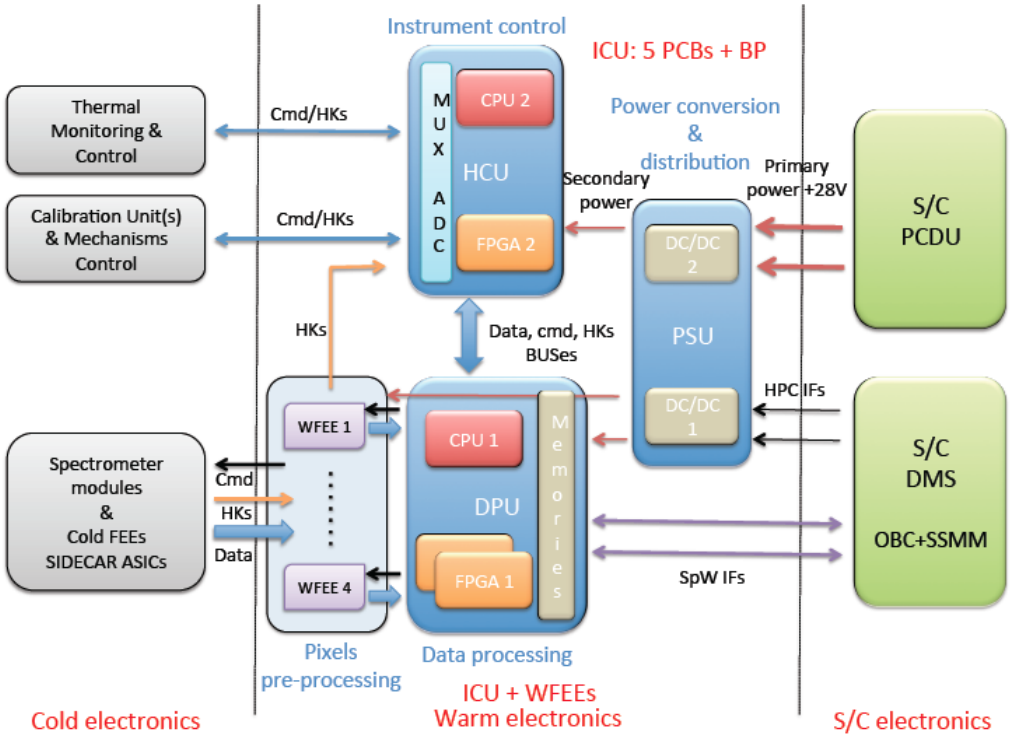

Fig. 11 – EChO payload electrical architecture block diagram (baseline solution).

ICU is mainly a digital unit with processing and data buffering capabilities interfacing both the spacecraft electronics and the digital section of the payload warm front-end electronics for commanding, data and housekeepings (HKs) acquisition, A/D conversion and dispatching, data packetisation and spectra pre-processing, as well as providing finely regulated voltage levels to all its subsystems and FEEs. Cold front-end electronics ASICs send digitised data and analog HKs (TBC) to WFEEs for packetisation in CCSDS format before sending them to the ICU by means of N+R Spacewire (SpW) links.
A Data Processing Unit (DPU), a HK and Calibration Source Electronics (HCU) and a Power Supply Unit (PSU) are the main blocks of the ICU, as schematically represented in Figure 11 and 12 (the latter as

alternative solution without using WFEEs).
The currently adopted ICU architecture interfaces 4 warm front-end electronics communicating with an on-board ICU digital subsystem with processing capabilities, the Data Processing Unit (DPU) and the Housekeeping and Calibration source Unit (HCU) both based (as baseline) on a rad-hard space qualified processor and devoted, respectively, to the *Data Processing Function* and to the *Instrument Control Function*. Both processors (CPUs) run the main Application SW suitably designed to perform separately the two functions, to manage the payload operating modes (instrument managing) and the overall data acquisition procedures and processing.
This architecture also presents the advantage to be compliant to a possible split of responsibilities and test and AIT/AIV procedures as well as EGSE provision between two different institutions respectively in charge of the data processing task and the instrument control task.

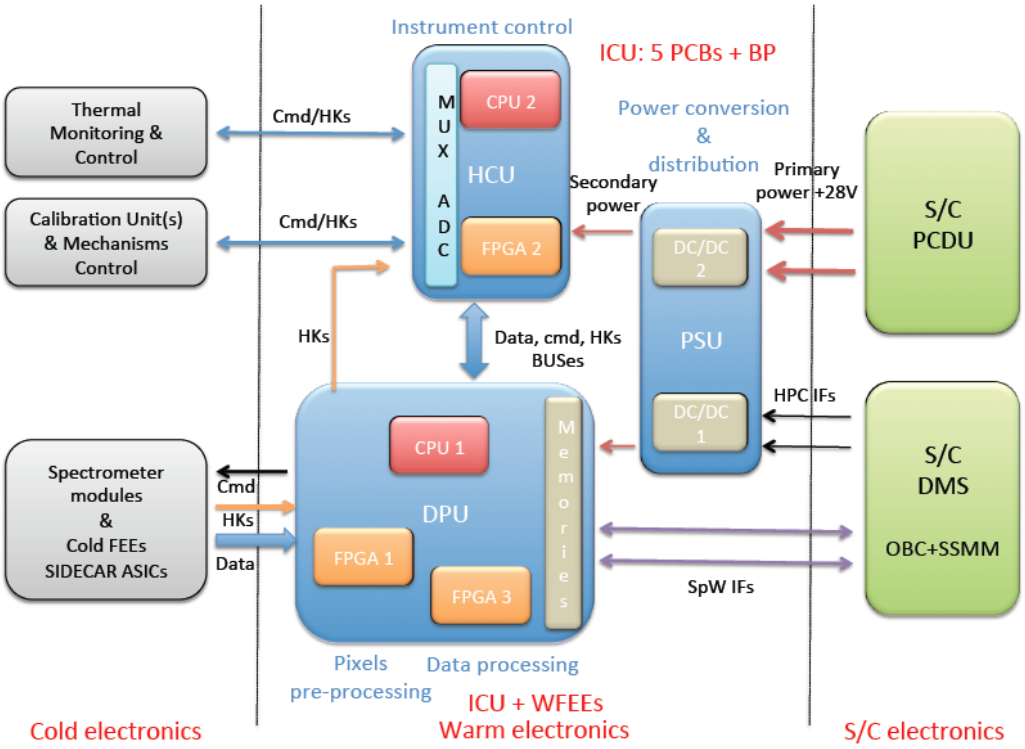

Fig. 12 – EChO payload electrical architecture block diagram (alternative solution).

The data processing function at pixel level will be supported by two rad-hard FPGAs working @ 80 MHz (assumed frequency for the processing resources evaluation) acting as co-processors to perform on-board (HW implemented functions) pixel-based data processing procedures.
The DPU will implement the digital data processing, the data storage and packetisation, the telemetry and telecommand packets handling and the clock/synchronization capability to temporally correlate the scientific data coming from the different spectrometer channels. A single common TM/TC interface is foreseen to minimize and simplify the number of interfaces towards the spacecraft.
As baseline, DPU is composed by a processing board hosting the scientific digital data processing CPU and the two ancillary FPGAs working as a co-processors and a memory board hosting all the memories needed to load and run the Application SW (PROMs, EEPROMs and SRAMs) and buffer the incoming scientific data (SDRAMs or FLASH – TBD) prior digital processing and data formatting. Memories addressing functions could be performed by one of the two FPGAs that will also acts as a memory controller for data buffering.
DPU and HCU will host and share an internal PCI interface to the PCI bus including data, address and control buses. Alternatively an AMBA bus could be used (TBD/TBC). The PCI bus is connected to the rad-hard processors (an ITAR-free LEON2 AT697F or a LEON3 from ATMEL running @ 60 MHz were considered, as baseline, to evaluate the processing and instrument control power needs) and to the main digital logics hosting a PCI I/F.
ICU manages both processors and logics to perform all the required tasks as digital processing (pixels

sum, average, digital binning, windowing, spectra cropping and masking, pixels deglitching -if needed TBC/TBD-, data and HKs compression) and memory management.
A Power Supply Unit (PSU) will distribute the secondary voltages to the instrument subsystems by means of rad-hard DC/DC converters whereas the HCU will provide instrument/channel thermal control, calibration sources, mechanisms (TBC) and HKs management.
PSU will be feed by two (N+R) +28V power interfaces and will be equipped with two (N+R) BSMs (Bi-Levels Switch Monitors) to report to the S/C the unit status (switched ON/OFF) as defined by two Main (ON/OFF) plus two Red (ON/OFF) High Voltage - High Power Pulse Commands (HV-HPC) with interface characteristics as defined by ECSS standards.
DC/DC converters are hosted by two boards of the PSU in order to feed all the ICU subsystems and provide the basic voltage levels to the WFEEs, so the present ICU design foresees as baseline 5 Extended Double Eurocard (233.4 mm x 220 mm) electronics boards in a fully redundant architecture aboard the same PCBs in a cold strapped configuration exploiting the ICU back panel board interfacing all the electronics subsystems. The ICU redundancy policy is based on a trade-off solution removing or reducing to an allowed level the impact of any single-point failure thanks to its cross-strapped fully cold-redundant architecture.
Table 4 reports the ICU daily data volume, the data rates to the S/C, the CPUs expected processing power and memories usage. The followings assumptions have been taken into account: the averaged number of clock cycles/elementary operation is 3 (1 MIPS = 3 M clock cycles); the number of elementary operations/pixel take into account the OS background activity overhead; digital data are stored in memory (SRAM and SDRAM) by a FPGAs before CPU processing; masking is performed by a FPGA aboard WFEEs before making data available to the CPU; payload control refers to TC activity between ICU and the 4-channels instrument including calibration units management. Once pre-processed scientific data are temporarily buffered and sent immediately to the DMS Solid State Mass Memory.

Scientific channel:	VNIR	SWIR	MWIR-1	MWIR-2	LWIR
Detector Frame Format	512x512	1024x13	63x13	87x13	50x6
Pixel pitch (µm)	18	18	25	25	25
Binning	5x5	1x1	1x1	1x1	1x1
Digital masking	70%	100%	100%	100%	100%
# bit/pix	16	16	16	16	16
Primary rate (Hz) - Bright targets case	8	8	8	8	8
Ramp lenght (s) - Bright targets case	3	3	3	3	3
# Samples per ramp	24	24	24	24	24
Housekeepings TM (Gbit/day)	0.2				
Efficiency (R-PERF-060)	85%				
Contingency (EID-A R-2430)	50%				
Available ossless compression factor (CR)	2÷2.5				
# CPUs (LEON-like running @ 60 MHz)	2 (Processing & Instrument Control)				
# FPGAs (RTAX 2000-like running @ 80 MHz)	3 (Px pre-processing, memory manag. and aux fnc)				
SRAM needed (MBytes)	16 (8 x 2 banks)				
SDRAM needed (MBytes)	20				
EEPROM/PROM (MBytes) - BOOT SW, BIOS SW, ASW	8 (4 x 2 banks)				
Daily averaged data rate	< 60 kbit/s				
Peak data rate (burst mode, if needed)	< 10 Mbit/s				
Science TM (Gbit/day)	< 5				
TOT. expected daily data volume – science + HKs (Gbit/day)	< 5				

Tab. 4 – ICU processing power, data rate, data volume, required amount of memories.

Note: *Table 4 values strongly depend on data processing required for on-board (ICU) deglitching procedures, compression task and pixels pre-processing. Presently pixels deglitching is foreseen to be operated on-board but could be avoided given the short integration times for bright targets and the very low likelihood of cosmic rays hits on pixels (ref. Technical Note IAPS/ECH/TN/01-013, Issue 0.1).*

Our basic assumption is that we sample up-the-ramp pixels in a non-destructive manner with a relative high rate sampling (presently up-to 8 Hz). There will be destructive readouts after some seconds (integration times for bright, normal and faint sources) with the length of the ramp determined either by the saturation limits of the detector for a particular target – determined during operations planning – or by experience of the maximum length of a ramp allowed before a cosmic ray hit. This will be determined by in flight tests and calibrations and on-ground simulations activities. The highly sampled ramps are then fitted and the pixels photocurrent extracted. These data will then on-board processed also for pixels deglitching by cosmic rays (as baseline), lossless compressed and transmitted to the S/C.
The ICU will carries out all communication and commanding tasks of the instrument. It will also serves as the central data-handling unit. Incoming science data will be processed, compressed and formatted in CCSDS format according to the operating mode.

All the ICU processing and buffering capabilities are presently evaluated taking into account a 50% of margin, as usually adopted at the ending of the Assessment Study (Phase A) and as reported by EID-A R-2430.

4.1.1 On-board data processing

The most demanding module from the point of view of digital processing are the SWIR and the VNIR one as the latter is based on a MCT panoramic detector composed by 512 x 512 - 18 μm pixels as baseline, or 512 x 512 – 15 μm pixels as an alternative choice (Selex device). In order to perform on board DPU data processing and pixel deglitching from cosmic rays hitting the VNIR FPA before digital pixels binning (on-chip binning is also possible, as baseline) to produce spaxels[1], the two FPA halves will be digitally masked and cropped rejecting all pixels hosting no VIS and NIR spectra information, reducing the overall pixels number to be processed by masking to about 70% of the entire array. Digital masking and image cropping will be performed aboard WFEEs FPGAs (TBD/TBC) in order to reduce the overall DPU processing load. The EChO payload digital processing is therefore a distributed digital processing.

4.1.1.1 On-board processing steps

All detectors will be read non-destructively and periodically reset after a certain number of samples have been acquired. The length of the reset interval will be adapted to the brightness of the source. The ramp-fitting implementation used in this study does assume uniform sampling and samples grouping if needed to save processing and reduce data volume (up-the-ramp multi-accumulation sampling).

Before operating individual pixel processing it will be performed (TBD, channel by channel) detector windowing and/or array digital masking and/or image cropping respectively at detector level and WFEEs level in order to limit the effective number of pixels owning to the produced spectra to be successively processed by WFEEs and ICU.
At the beginning of the procedure, basic corrections will be applied to individual pixels, while after the binning each spaxel (VNIR case) is processed individually.

The main processing steps as illustrated in Figure 13 (mostly for the VNIR channel one, but useful also for all the other channels) are:

- Bias correction: an internal bias is subtracted to bring all samples to the same “ground”. This is necessary for later binning of the data down to spaxel resolution;
- Pixel reordering: pixels are extracted from the serial stream in output from the readout electronics and reordered, bringing them into a more suitable order in memory for subsequent data processing steps. History and average buffers with ancillary data can be formed at this level;
- Saturated pixels identification and rejection: by defining a cut-off value for the upper limit of the linear region of the detector’s response curve;

[1] Spaxels are defined as nxn binned pixels along the spatial and spectral dimensions.

- Responsivity correction: correction based on radiometric calibration, thanks to an array responsivity map, will be applied if necessary;
- Spatial and spectral pixel binning to build spaxels;
- Temporal samples co-addition: depending on the ramp fitting algorithm, “scans” and “groups” have to be formed (*m* scans per group) if needed;
- Rejection of the data that don’t satisfy the noise requirement at beginning of the ramp, when necessary;
- Non-linearity correction: if necessary, the ramps will be linearized, even during the multi-accumulate processing);
- Progressive *linear least square fit* to calculate ramps slope (pixels/spaxels photocurrents);

  Note: The above four steps could be necessary to decrease readout noise to specifications. Frames in a group must be contiguous and in the number necessary to reach the required total noise performance limit after co-addition (assuming a multi-accumulation readout mode). These processing steps must run at the spaxels readout speed. Using a fixed very simple parameterization (to be optimized during calibration and algorithm tuning procedures on ground), it can be conveniently performed in hardware.

- Cosmic rays and other glitches identification (TBC/TBD): proper glitch detection and rejection strategies will be implemented, if necessary, with a proper algorithm still to be defined;
- Bad spaxels correction and linearization;
- Frame generation: processed science frames created here will be received on ground;
- Frame buffering;
- Lossless Compression (compression of the data to save data volume and bandwidth);
- Packetisation according to the required TM format: all data products will be packaged;
- Storage in mass-memory (SSMM) and scheduling for transmission.

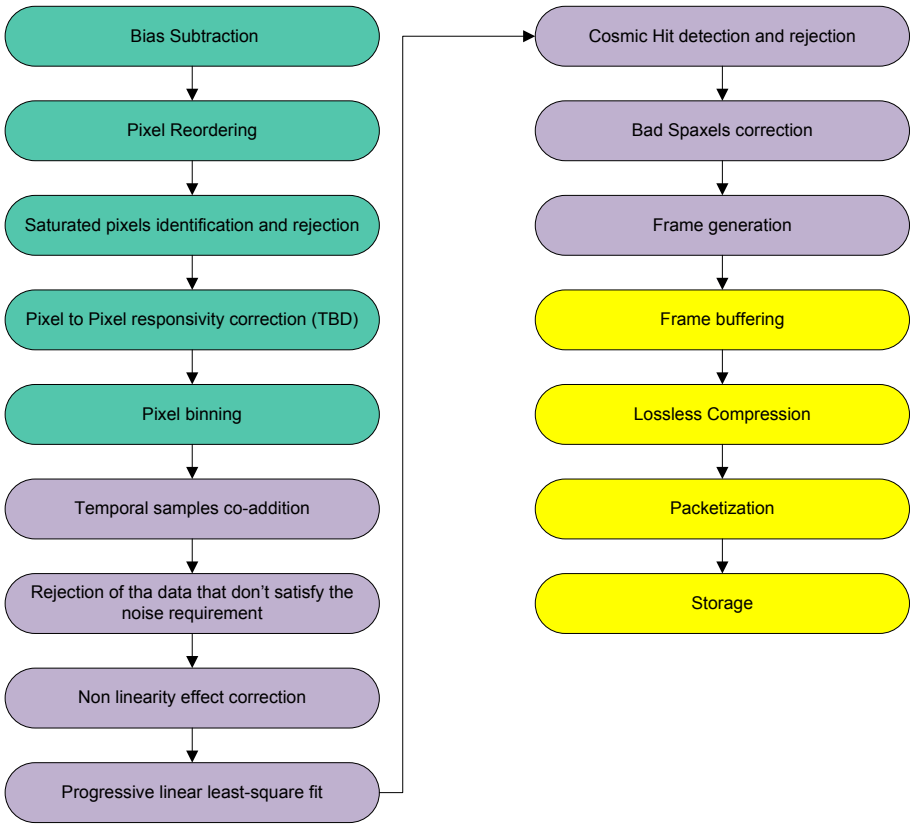

Fig. 13 - Scheme of the data processing steps: green blocks refer to pixel pre-processing activities; purple blocks refer to processing steps at spaxel level and yellow blocks identify frame level processing activities.

The listed steps refer to the processing of a single focal plane spectrometer. It is a standard on board processing chain, see for example Offenberg et al. 2001 and 2005, Bonoli et al. 2012, and a parallel processing of more than one instrument operating simultaneously at the focal plane should be taken into account.
The final overall processing of EChO data will be defined during Phase B and tailored for each one of the focal plane spectrometers. Dedicated simulated data flows will be used to verify the effectiveness of the data reduction steps. In particular the deglitching algorithm performances should be verified against the expected data redundancy, the data acquisition rate and the spaxels dimensions.
Finally, the need to implement lossless compression on-board is strictly related to the results of the on-board deglitching study. If confirmed, a dedicated trade off activity to evaluate the performances of different standard lossless compression algorithms on the on-board CPU processor should be planned.

4.1.1.2 Pixel deglitching

Deglitching detectors pixels arrays from cosmic rays hits is commonly an operation to be performed basically at pixel-level. Operating binning on-chip (e.g. on-board the VNIR detector ROIC) would lead to lose any pixel-based info on cosmic rays hits that would blur the spaxel integrated signal at the same time.
Taking into consideration the predicted cosmic rays flux for JWST-MIRI instrument and an integration time from 1.5 two 3 seconds for bright targets only less than 0.02% (ref. Technical Note IAPS/ECH/TN/01-013, Issue 0.1) of pixels would be interested by cosmic rays hits, so an option to be considered could be discarding any on-board deglitching operations based on pixels processing at least for bright targets.
The classical deglitching pixel-based procedure is a demanding processing task for the DPU CPU that would require the heavy use of the processor FPU (Floating Point Unit) for the second derivative calculus needed for the glitches recognition and correction. Probably it would be better to perform deglitching at "spaxel" level (i.e. 36 px/spaxel for the VNIR channel one) by detecting cosmic rays hits and discard them as outliers w.r.t. e.g. a median operation performed on sub-arrays. Pixels affected by cosmic rays hits should be flagged and not considered for the rest of the ramp production but properly replaced. In this manner we should avoid heavy processing tasks, like the derivative calculus and a heavy FPU use. A possibility to be explored could be to perform this kind of simplified deglitching procedure at FPGA level (HW-level).
The number of pixels owning to a spaxel and affected by a cosmic ray hit should be determined by the hit geometry and particles energy. They likely would affect mainly the detector array through the direction parallel to the optical axis and the angle defined by the optics F/# and buffles. So just few pixels should be interested by a single cosmic ray hits and it should be possible to operate deglitching only for the faint targets (if needed) which require longer exposition times with a bigger and not neglecting hit likelihood.
Deglitching from cosmic rays hits has surely a big impact on the overall ICU processing architecture and should be carefully evaluated in respect of the overall system budgets. Deglitching is presently foreseen at CPU level in the ICU processing needs evaluation procedure (see section 4.4.5).

4.1.1.3 Data compression

Once performed pixels and spaxels on-board processing all the scientific data defining spectra (ramps slopes defining pixels/spaxels photocurrents) will be compressed, prior sending them to the OBC SSMM to be stored and suitably formatted in order to send them to ground. The present compression task takes into consideration Rice or Smallrice algorithms that are written in C, C++ and/or assembler for the most demanding sub-tasks. The foreseen lossless compression ratio (CR) is presently estimated to be between 2 and 2.5.

4.1.2 ICU budgets

The ICU power, mass and volume budgets are reported in Table 5. The present overall dimensions are not considering the box mounting feet.

Description	Basic (EID-A R-1880)	Nominal (with 20% contingency) (EID-A R-1890)	Margin (EID-A R-1910) (EID-A R-0570)
Power	20 W	24 W	0
Mass	7.5 kg	9 kg	Tot. electr. < 25 kg
Volume	250 x 240 x 150 mm^3	-	0 x 0 x 30 mm^3

Tab. 5 – ICU budgets.

4.1.3 Electrical IFs to the S/C

The ICU is interfaced to the SVM OBC and SSMM through a +28V power line (Nominal + Redundant), two discrete high voltage - high-power command line HV-HPC (N+R) for switching on/off the unit and a (N+R) Spacewire (SpW) interface for commanding, HKs and data transfer to the OBC (see Figures 14 and 15). The SpW interfaces are implemented inside the DPU service logic FPGA as an IP core that, in turn, is bridged to the PCI bus or the AMBA bus (TBD/TBC). The same FPGA or a dedicated FPGA (TBD/TBC) controls also the Buffer Memory section used to store data for digital processing and as a temporarily buffer before sending them to the OBC.

4.1.3.1 Power IFs

Nominal Power Supply and control:

- Power line: 28V + RTN (From S/C PCDU to ICU)
- Switch On HPC (Signal + RTN) (From S/C DMS to ICU)
- Switch Off HPC (Signal + RTN) (From S/C DMS to ICU)
- Switch Status BSM (Signal + RTN) (From S/C DMS to ICU)

Redundant Power Supply and control:

- Power line: 28V + RTN (From S/C PCDU to ICU)
- Switch On HPC (Signal + RTN) (From S/C DMS to ICU)
- Switch Off HPC (Signal + RTN) (From S/C DMS to ICU)
- Switch Status BSM (Signal + RTN) (From S/C DMS to ICU)

MIL1553 BUS use is TBD/TBC and could be exploited e.g. to interface the Fine Guidance System to the S/C.

4.1.3.2 TM/TC IFs

Nominal I/O digital data interface:

- Standard Spacewire link (configured @ 10 Mbit/s – TBC); From S/C DMS to ICU

Redundant I/O digital data interface:

- Standard Spacewire link (configured @ 10 Mbit/s – TBC); From S/C DMS to ICU

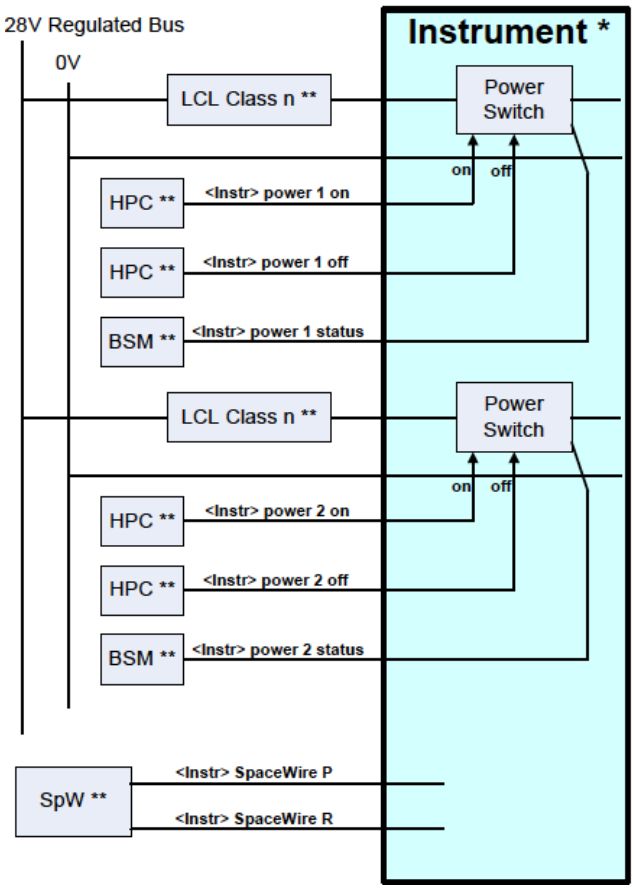

Fig. 14 – Electrical IFs between SVM and the instrument.

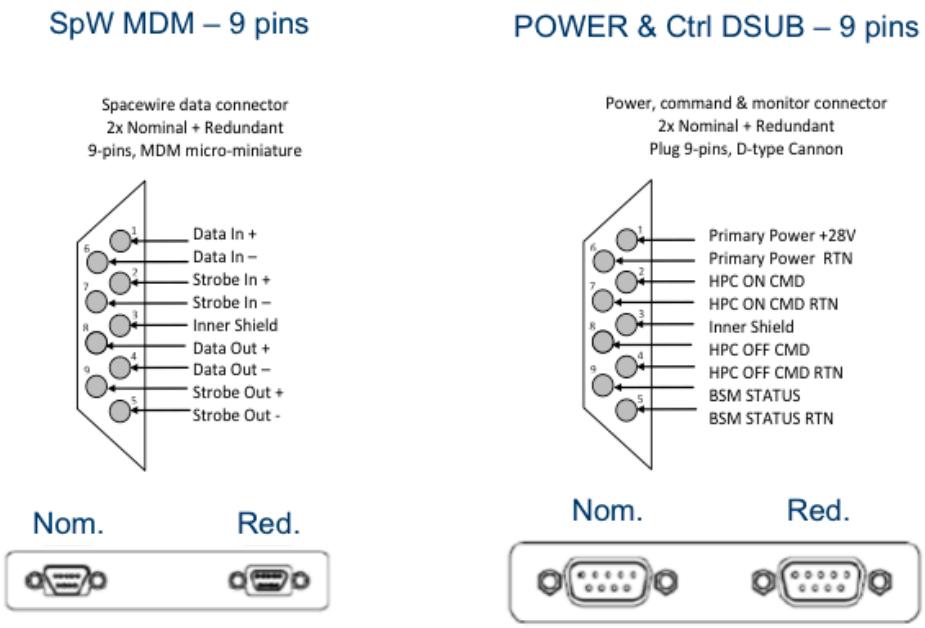

Fig. 15 – TM/TC communications IFs and Power IFs.

4.1.4 Electrical IFs to WFEEs

Electrical IFs to the WFEEs are represented by a nominal and a redundant SpW link (or LVDS link TBD/TBC) for every module in order to transmit digital data and HKs telemetry and telecommands (ref. Figure 15). Other analog IFs could be implemented in order to transmit to ICU analog HKs to be multiplexed and digitised by the HCU unit (TBD/TBC).

4.1.5 Grounding

EChO EID-A document states that “the PI shall develop an instrument EMC Control Plan according to ECSS-E-ST-20C and the Prime Contractor will ensure that a controlled grounding and isolation concept will be defined for the spacecraft prior to initial release of the EMC control plan. The PI shall be compliant with the grounding and isolation concept defined by the prime contractor”.
Waiting for the Prime Contractor grounding concept, the EChO ICU present grounding concept is the Distributed Single Point Grounding (DSPG) one (see Figure 16), involving all the 5 ICU electronics boards.

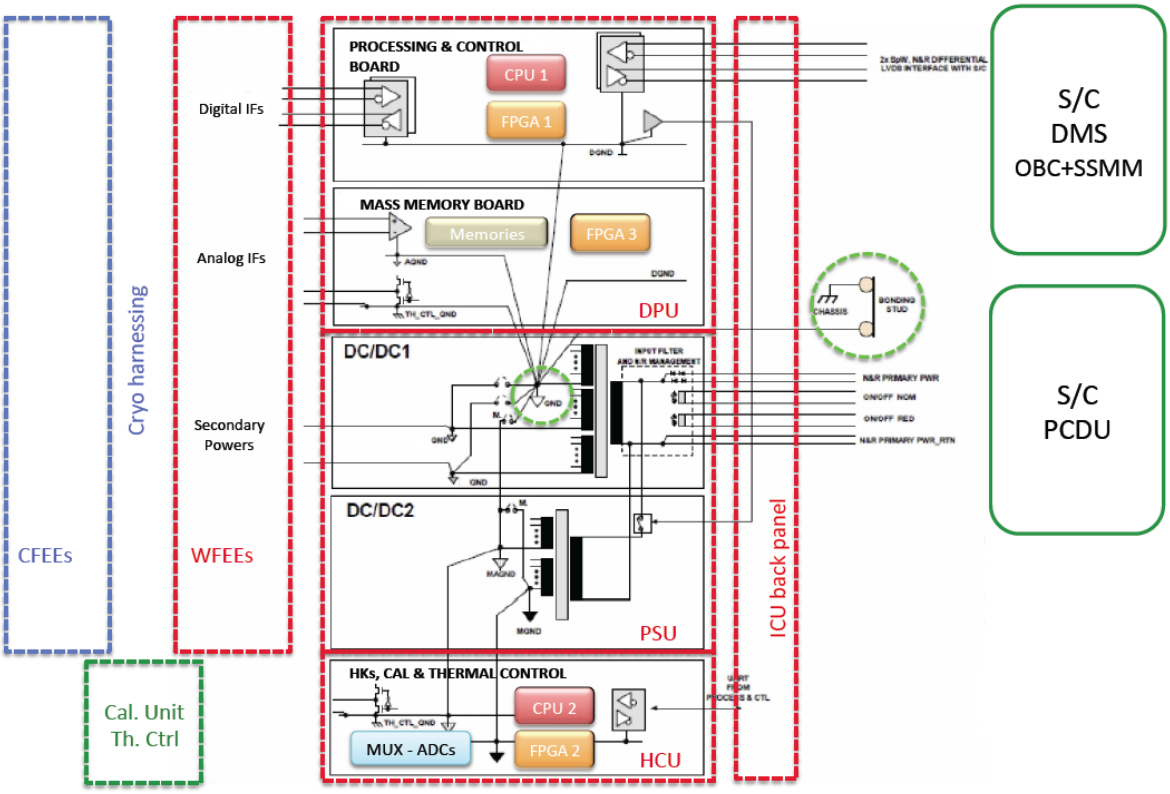

Fig. 16 – ICU grounding concept.

4.1.5.1 Grounding and Isolation

The principle is to realize a single point ground for each independent power network and to provide isolation between those networks (Figure 16 and 17). In order to match this goal, any primary power and return input lead of equipment shall have a DC isolation of at least 1 MOhm (shunted by no more than 50 nF) to equipment chassis and between power input lead and secondary power leads.
In order to avoid grounding loops, secondary power distributed inside the equipment shall be galvanically insulated and decoupled by DC/DC converters.

4.1.5.2 Bonding and Charging Control

ICU box will be bonded to the platform bench via its mounting feet. In addition, the unit shall provide a bonding stud/hole for bonding via a bond strap. All “sensible” surfaces will be treated to be electrically conductive, in order to mitigate and control charge accumulation phenomena.

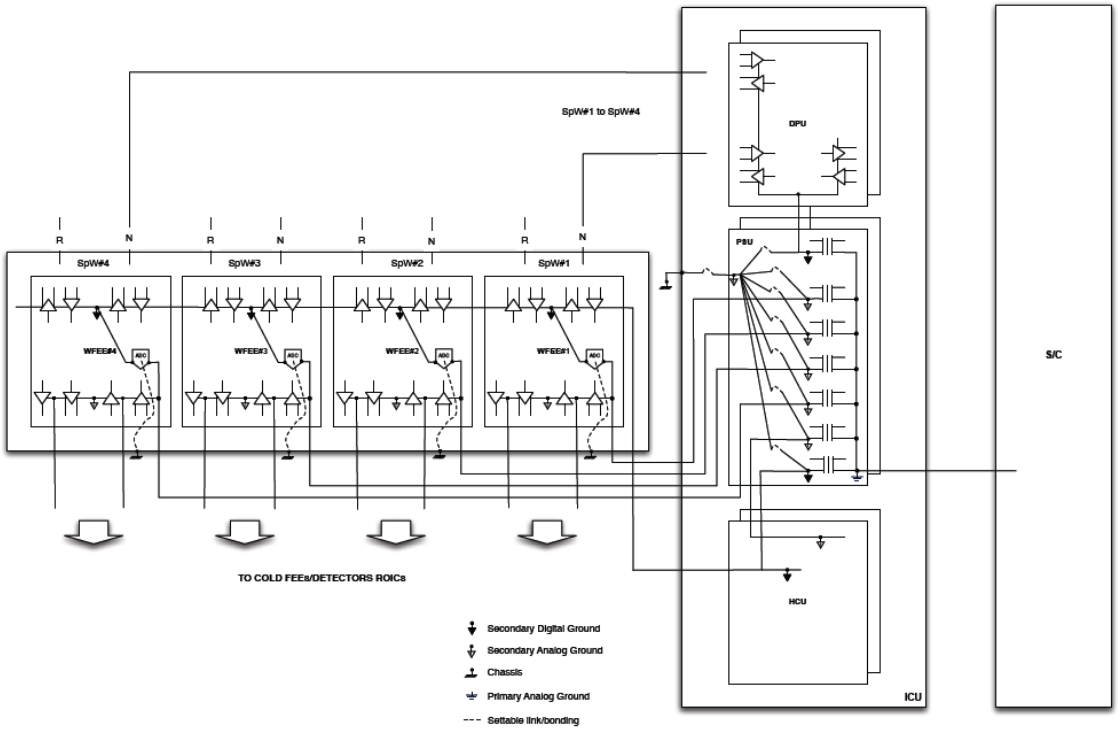

Fig. 17 – ICU and WFEEs grounding scheme. ADCs inside WFEEs are used (TBC) to convert analog HKs to be sent to the ICU.

4.1.6 Mechanical design

The ICU basic mechanical design is represented in Figure 18. The ICU box dimensions are 250x240x150 mm^3 mounting brackets and feet excluded. All the electronics boards are fixed by means of space qualified card lock retainers and are reinforced by an aluminium structure hosting the connectors as depicted in the figure.

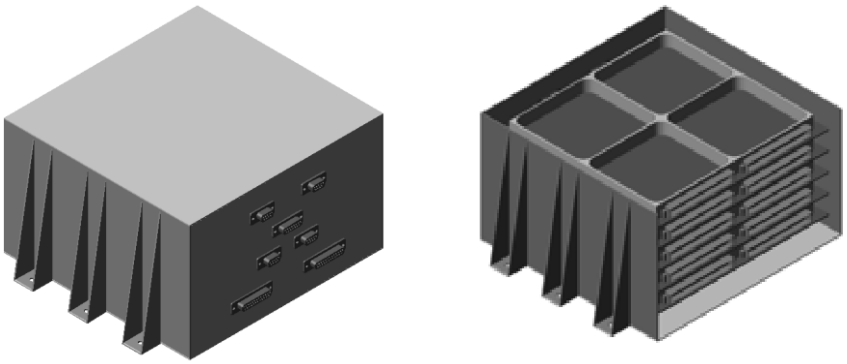

Fig. 18 – ICU mechanical design.

(connectors # and location are TBD/TBC and for illustration purpose only)

The ICU box, made by aluminium alloy, will be provided by an external bonding stud to connect analog and digital grounds to the unit chassis, as a possible configuration for testing and external noise shielding.

4.1.7 Thermal design

The ICU thermal design is based on a simple radiative and conductive heat transfer analysis performed on similar units, that lead to the overall thermal load dissipation to maintain all the electrical components in their operational and survival ranges and will be refined during the Definition Study (Phase B) of the project. Thermal straps could be foreseen inside the unit to manage properly heat flows between hottest components and the ICU chassis.

4.2 HARNESSING

We assume that the models followed by Herschel, Planck and JWST are used regarding the provision of the harnessing between the S/C Service Module and the EChO Payload Module. This leads to a split in the responsibility for the instrument cryo-harness between the Consortium (for all harnessing on the IOB and within the instrument modules) and ESA/Prime who we assume will provide the harnessing between a bulkhead on the PLM to a connector panel on the SVM.
The consortium would provide the detailed electrical performance specification for this harness, but since the routing and thermal control aspects will be wholly under control of the spacecraft provider we assume that these harnesses are provided by the Prime. This assumption can be discussed further if necessary during the following phase.
ICU IFs harnesses will be divided into EMC classes and will follow the guidelines provided by the platform Prime respecting the unit budgets. All cabling will have an overall screen to provide an EMC shield against radiated emissions and susceptibility and to avoid charging of the cabling dielectric materials. No flying harness is foreseen -as baseline- inside the ICU. Cryogenic harnesses from WFEEs to CFEEs is TBD. No harness dielectric will be directly exposed to space plasma environment.

4.3 ELECTRONICS SIMULATOR

The electronics simulator (ref. ECHO-IAA-SP-0001) is intended to provide an independent functional platform for testing and simulations. Its main purpose is to simulate the behaviour of the ICU operating on board the EChO payload, providing useful data and metrics to analyse and monitor sensors, FEEs electronics and ICU performance.
The present simulator (Figure 19) provides TM and HKs acquisition and is virtually controlling two emulated devices retrieving randomly generated data. This setup serves as an early testing environment and letting the team test debug and improve the simulator in lack of real devices.
The development of the simulator is based on a FPGA, which manages all housekeepings, telecommands and telemetry data. All the acquired information is sent to a computer via Ethernet connection for further analysis. The board containing the core of the simulator is GR-XC6S, manufactured by Pender Electronics (Figure 20). The FPGA model is a Xilinx Spartan-6 XC6SLX75.
ICU simulator consists of four modules: one for H/W interfaces (red box) and the three remaining ones make up the S/W architecture (violet boxes: simulation, control and monitoring and user interfacing). From this point of view, the system simulation is running the ICU components loaded and provided by the control module, which is also in charge of stand-alone monitoring of every parameter of the system and it's operated through the user interface, providing the user with the whole needed functionality for practical operation, configuration and inspection of the simulation system.
The FPGA integrates an IP core of LEON3 processor. The simulator application running on the development board is coded in C++ and controlled by RTEMS, a fully featured and open-source real-time operating system widely used in embedded platforms.
The software architecture is based on two main components, Device Manager and HK Manager, controlling Device data acquisition and HKs sensor sampling, respectively. Everything is coordinated by a Core component, in charge of TC reception and TM retrieving, and responsible for communication

between managers and users.

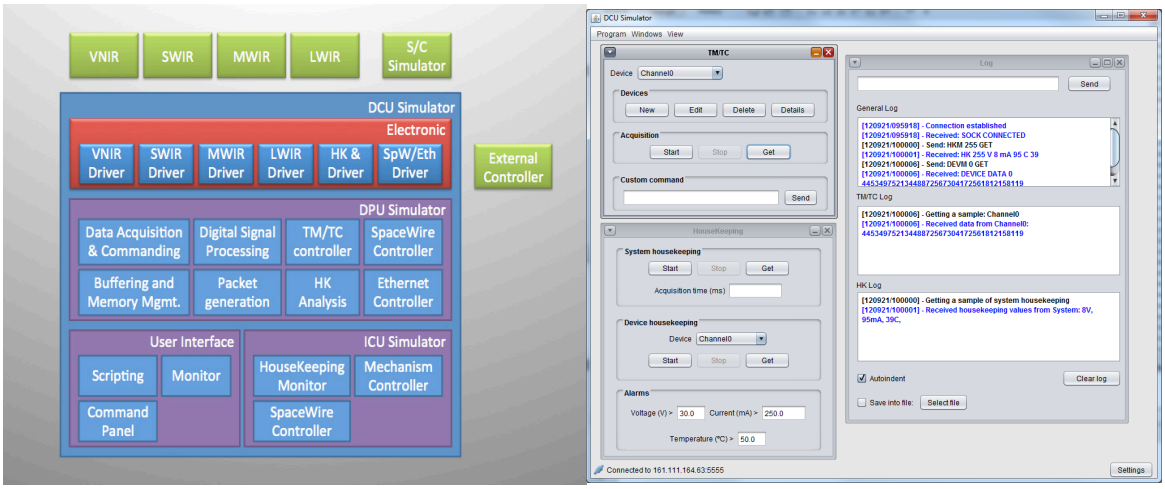

Fig. 19 – ICU simulator (SW interface).

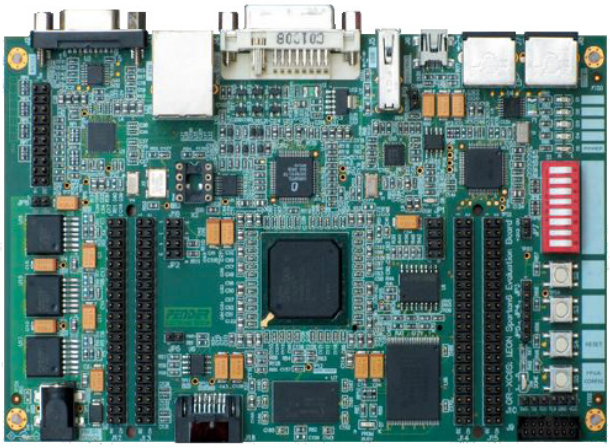

Fig. 20 – Electronics board containing the SW/FW core of the simulator.

4.4 SOFTWARE DESCRIPTION

The EChO Payload instruments On Board Software (P-OBS) running on the ICU will be composed by the following main blocks:

- *Boot Software:* it is installed in the PROMs of ICU board and allows loading the ICU application software. It contains all the low level drivers for the CPU board and its related interfaces.

- *Instrument Control Software:* it refers to the software performing the operations of the EChO scientific payload. It implements the data-handling functions of the payload, manages the spectrometers operating modes and runs autonomous function. It implements the interface layer between the S/C and the instruments operation.

- *Data processing Software:* implements the ICU science data on-board processing and lossless compression (i.e. RICE). It implements the data packetisation for the transmission to the S/C Solid State Mass Memory (SSMM).

4.4.1 EChO On-Board Software functional analysis

The EChO ICU is responsible for the following main activities:

1. Telemetry and Telecommand exchange with the S/C CDMU;
2. Instrument Commanding, based on the received and interpreted TCs;
3. Instrument monitoring and control, based on the Housekeeping data (HKs) acquired from the focal plane instrument units;
4. Synchronization of all the scientific payload activities;
5. Detectors readout data acquisition, pre-processing and formatting according to the selected Telemetry protocol;
6. Science Data download towards the S/C Mass Memory.

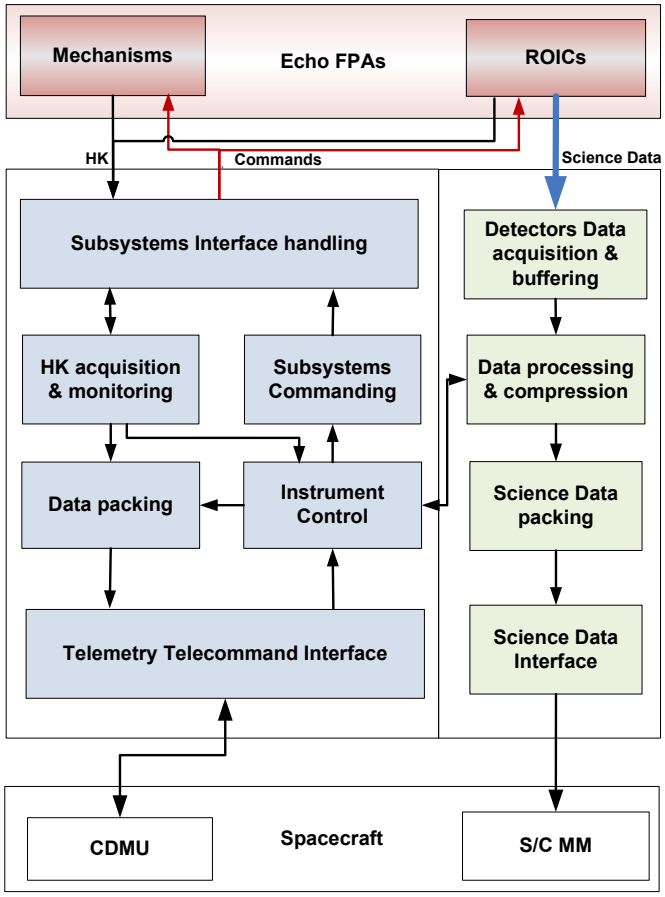

Fig. 21 - ICU OBS functional components block diagram.

These activities can be grouped into the *Instrument Control* and *Data Processing* software: these two SWs will constitute the On Board Software (OBS) of the EChO science payload (P-OBS). The On Board Software will be implemented as a real-time multitask application.
The Block Diagram reported in Figure 21 shows the main ICU functional components. The two different colors indicate the different groups of functionalities of the Instrument Control and the Data Processing software.

4.4.2 Software layers

The EChO Payload instruments On Board Software (P-OBS) layers structure is presented in Figure 22. The boot software component refers to the start up software described in the previous section: it is installed in the PROMs of the ICU boards and allows for the application software loading. It contains all the low level drivers for the CPU and its related interfaces.

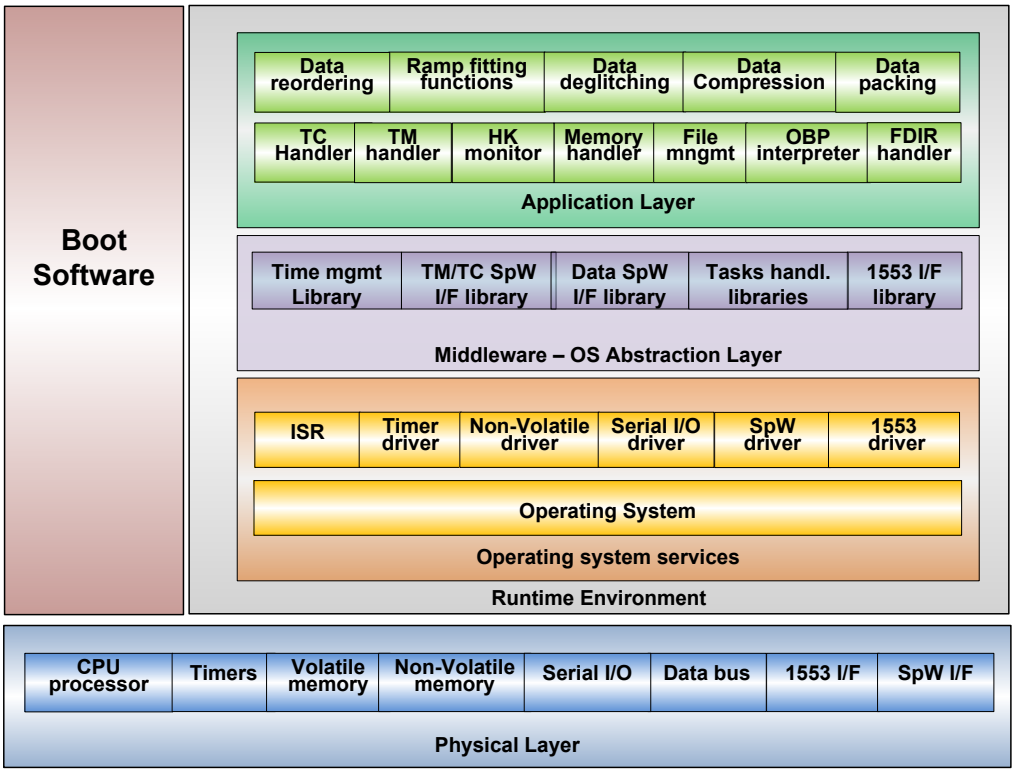

Fig. 22 - SW layers structure of the EChO Payload instruments On Board Software (P-OBS).

The physical layer includes all ICU HW components with a direct level of interaction with the on board software. In particular, the considered baseline CPU is a LEON processor. It is a 32-bit SPARC-compliant processor, which results from ESA's efforts in the development of processors for space applications. It will be used in several space missions (e.g. the Swedish PRISMA mission, the European Space Agency Proba-2, GAIA and Bepi-Colombo missions) and it is planned to use it also in a number of medium size missions competing in the frame of the ESA Cosmic Vision program.
The Runtime environment includes the Real Time Operating System (RTOS) layer, necessary to provide multi-tasking support. In case the baseline architecture based on the LEON processor will be confirmed, the RTEMS operating system is a good RTOS candidate, being already used for applications on board ESA satellites. The other indicated operating system services include the drivers for the onboard memories, the onboard HW timers and the local data bus. The other OS services mentioned in the structure of Figure 22 are those not directly provided with the OS kernel.
An OS abstraction layer has then been included, in which all middleware libraries have been considered. The middleware services are based on the use of RTOS function calls. They include all library functions dedicated to the low level handling of the ICU HW devices/interfaces. All the middleware libraries will be developed in house and will provide a mean for developing an Application Software virtually independent from the HW and OS below it. This layer is very important and will ease the testing activities.
The Application Layer includes both the ICU instrument control software and the data processing software. The ICU instrument control software will implement the functions listed in points from 1 to 4 of the list in section 4.4.1: i.e. the TM/TC S/C interface handling, the payload housekeeping data acquisition and monitoring, the instruments operating modes management and the autonomous function execution. The software will be written in C++, though some functions may need to be coded in assembly to optimize their performance.

In case stringent timing requirements have to be met for subsystem commanding, an interrupt-driven command sequencer (On Board procedures, OBP interpreter) can be included into the ICU on board software. Based on the experience of Herschel's HIFI and SPIRE instrument control software, this is a flexible and effective solution to implement time-critical commanding procedures. Some preliminary tests on the performances of a simplified implementation of such a sequencer on a LEON 3 based SOC implemented on an FPGA development board (GR-XC3S-1500) have been already carried out. A 1 MHz timer has been used to trigger the highest priority interrupt of the system. Under normal work load conditions (only two tasks running, CPU load < 50 %), an average time jitter of the order of 1 us (for an overall test duration of more than 1 hour) has been measured, as expected. The proposed sequencer offers high flexibility and re-programmability possibilities, thanks to the straightforward way in which scripts can be reloaded during in-flight operation; this feature can be exploited to modify instrument control or measurement procedures in response to changed mission requirements. The sequencer is described in "*Di Giorgio et al. 2008"* and *"Liu et al. 2012"*.
The Data Processing Software implements all the necessary onboard processing functionalities, included the on-board lossless compression (i.e. RICE). After the compression the SW prepares CCSDS packets for the transmission to the S/C Solid State Mass Memory.

4.4.3 Boot SW

The boot software is stored in a PROM device, while EEPROM memory devices are used to store two or more images of the Application Software (On Board Software, OBS). The boot software is started automatically after the power on. The boot program is in charge of loading and starting the application program (OBS). A preliminary flow chart of the boot procedure is shown in Figure 23. The boot process is driven by command packets coming from the Spacecraft. The boot SW will be able to load and start:

- one of the OBS images stored in EEPROM (when the "boot from EEPROM" command is received);
- an OBS image received by means of specific commands; in particular, a series of memory management commands ("memory load") are used to store in RAM a complete new OBS image, which is then started at the reception of a "boot from RAM" command.

The boot procedure described above offers good reliability arguments because:

a) If the EEPROM is corrupted, the boot can still load an OBS image via "Memory Load" commands.
b) If any RAM cells in the area to be occupied by the OBS are broken, a new OBS image, which does not use that memory location, can be built on ground and uploaded via telecommands.

Of course there still remains the risk of a broken cell in PROM or in the portion of RAM used by the boot SW, which can lead to unrecoverable failures of the boot process.
The drawbacks of this procedure are:

a) Complex Boot program, it needs to handle the exchange of SpW packets (even if only a very limited set of packets is to be supported);
b) Big code size, it may be challenging to fit it into PROM device.

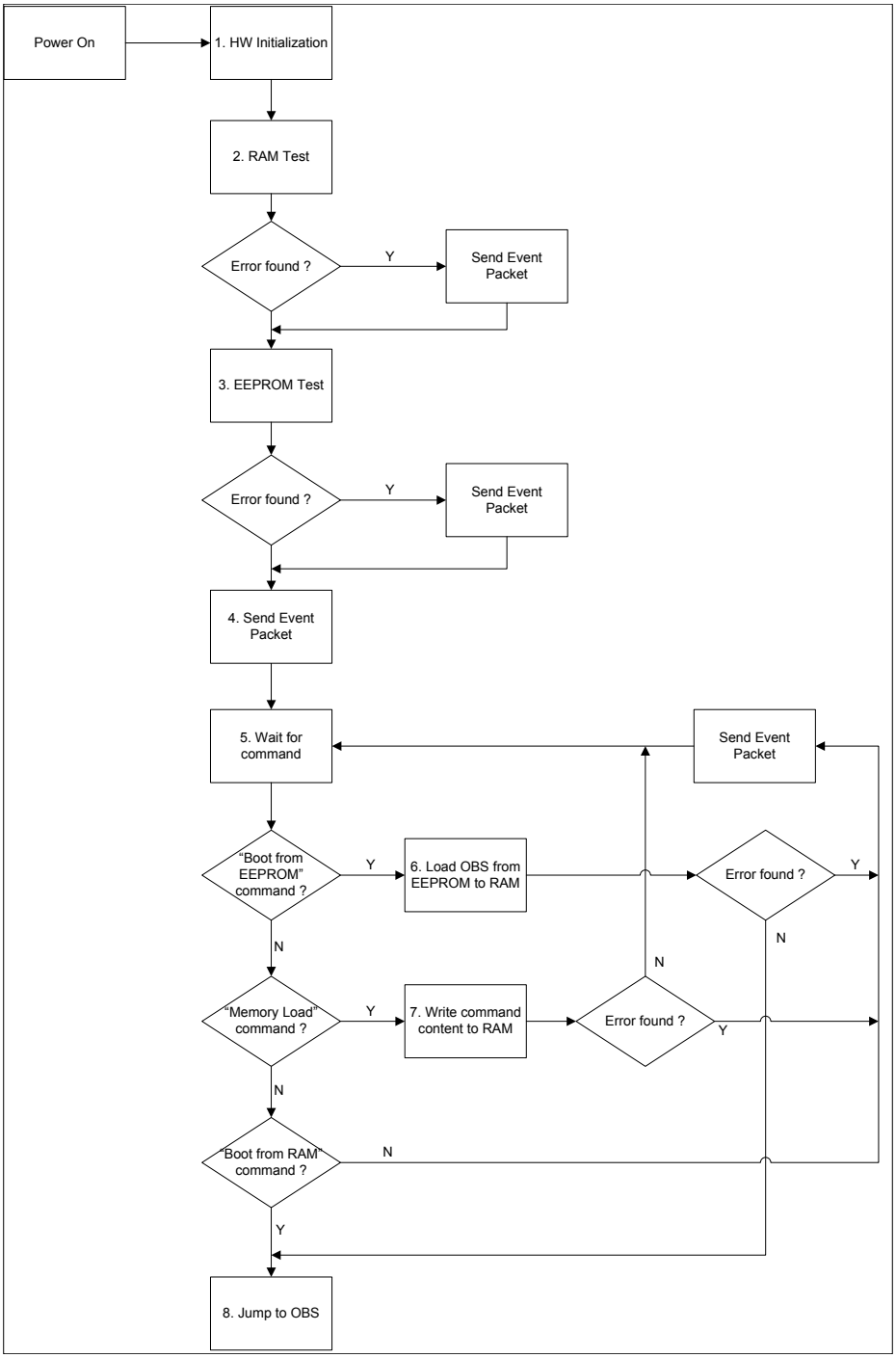

Figure 23 - Flow chart of the boot procedure.

4.4.4 Software project development life cycle

Given the EChO project constraints and planning, the *Incremental Life Cycle Model* is the most suitable to the OBS development.
In this model the requirements are almost all known at the beginning of the implementation phase of the project and can be divided into groups for incremental development. A core set of functions is identified in the first cycle and is built and deployed as the first release. The software development cycle is repeated, with each release adding more functionality until all requirements are met. Each development cycle acts as the maintenance phase for the previous software release. While new requirements that are discovered

during the development of a given cycle can be implemented in subsequent cycles, this model assumes that most requirements are known up front, which is the EChO case.
This life cycle paradigm has the following advantages:

- Provides some feedback, allowing later development cycles to learn from previous cycles;
- Requirements are relatively stable and may be better understood with each increment;
- Allows some requirements modification and may allow the addition of new requirements;
- It is more responsive to user needs than the waterfall model;
- A usable product is available with the first release, and each cycle results in greater functionality;
- The project can be stopped any time after the first cycle and leave a working product;
- Risk is spread out over multiple cycles;
- Testing may be easier on smaller portions of the system.

On the other hand, there is the disadvantage that the majority of requirements must be known in the beginning and that because development is spread out over multiple iterations, interfaces between modules must be well defined in the very beginning.
In the Incremental Life Cycle Model we intend to adopt, the following activities are included:

– software requirement & architecture definition;
– software design and implementation;
– software validation;
– software verification;
– software delivery and acceptance;
– software maintenance;
– software management process.

The activities to be performed in each cycle are represented in Figure 24.

The process will integrate reusable software from existing sources with newly developed software. Software design and coding will be performed by the *Software Development Team* using an object oriented design approach and generate class and object process interaction diagrams.
The software development activities will be logged into Software Engineering Notebooks and the unit tests results/tools will be made available to support management reviews, metrics calculations, quality audits, product evaluations, and preparation of product deliverables.
In each cycle, the reusable and new software units are integrated and tested, in accordance to the updated integration test plan.

Prior to delivery to system, a Test Readiness Review (TRR) will be conducted to verify readiness for system level testing.

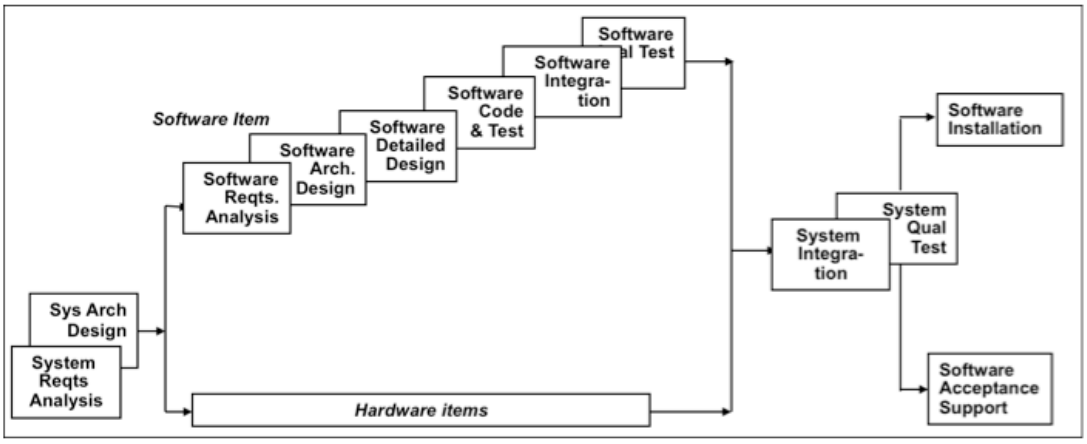

Figure 24 - OBS Software Engineering Process Model.

A Test Plan (TP) for a system level acceptance of OBS will be provided as output of the OBS Verification & Validation Work Package and approved by the EChO system team. The plan will be updated at each OBS delivery, in order to cover the testing of the new functionalities. The plan will be structured in test cases and will contain the related Test Description. The team (composed of system team representatives supported by OBS developers) that will execute the Acceptance tests will generate Problem/Change Reports (P/CRs) to describe software errors uncovered during test results analyses.
The separation of organizational entities and their testing responsibilities is illustrated in Figure 25.

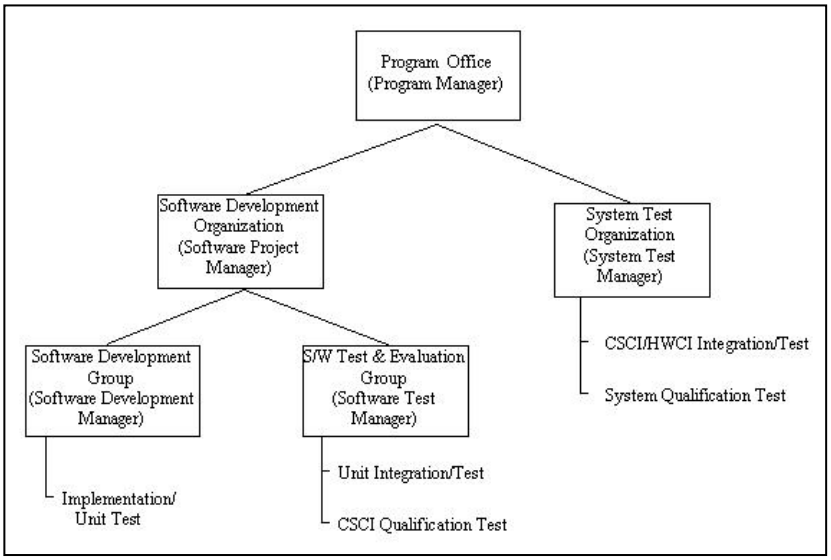

Figure 25 - SW development and testing team roles and responsibilities.

4.4.5 Processing power estimation

The CPU power required for the on-board processing (up-the-ramp fitting and deglitching -TBC/TBD- plus lossless compression) has been roughly estimated based on several assumptions on the total number of elementary operations needed for each one of the processing steps as reported in Table 6.

CPU's/FPGAs estimated % of occupation

		Bright Mode								
		Cycles/pixels or spaxels	Notes	Pixels, Spaxels, Ramps/s	Cycles/s	% CPU or FPGA	Buffers	Buffering sec	RAM needed 1s buffer [MByte]	
Pixels pre-processing TO BE PERFORMED ON HARDWARE! (FPGA)				Pixels/s						
Digital masking (in case of NO WFEEs use)		0	on FPGA	2099552	0	0	0	3	0.0	
Bias subtraction (substantially dark current subtraction)		18	on FPGA	1592502	28665043	36	2	3	19.1	
Pixel reordering		6	on FPGA	1592502	9555014.4	12	2	3	19.1	DPRAM to circular buffer
Saturated pixel identification and rejection		6	on FPGA	1592502	9555014.4	12	2	3	19.1	
Pixels responsitivity correction	move to CPU?	35	on FPGA and or CPU	1592502	55737584	70	2	3	19.1	
Pixel binning (spaxel construction)		15	on FPGA	183501	2752512	3	2	3	2.2	
Cosmic hits detection and rejection (simplified procedure for deglitching) on single pixels	really needed?	0	TBD on FPGA alg	1592502	0	0	2	3	19.1	
						133	(3 FPGAs)			
Samples or groups processing (# spaxels or pixels processed per unit of time)				Spaxels/s						
Temporal samples co-addition		12	only on VNIR spax	58720	704643.07	1.17	2	3	0.7	
Data rejection out of noise reqs		6		183216	1099297.5	1.83	2	3	2.2	
Non-linearity effects correction		9		183216	1648946.3	2.75	2	3	2.2	
Progressive linear least square fit (ramps slope evaluation)		40	RampFit (fast)	183216	7328650.2	12.21	2	3	2.2	cp + mask to RAM + rampfit
Cosmic hits detection and rejection (deglitching)	really needed?	220	TBD on algorithm	183216	40307576	67.18	2	3	2.2	
Bad spaxels and pixels correction		6		183216	1099297.5	1.83	2	3	2.2	
Frame generation		6		183216	1099297.5	1.83	2	3	2.2	
						88.81				
Compression, packetisation and storage				Ramps/s						
Frame buffering		4		7634	30536	0.05	2	3	0.1	
Lossless compression		60	smallrice	7634	458041	0.76	2	3	0.1	data from Roland
Packetisation		12	TBC	7634	91608	0.15	2	3	0.1	mostly the checksum
Storage		4		7634	30536	0.05	2	3	0.1	
						1.02				
Instrument control & OS overheads									19.1	maximum buffer size
Operating system and basic SW background activities overhead ~ 1 M clock cycles/s					1000000	1.67				
Instrument/scientific channels control ~ 1 M clock cycles/(s*channel)					5000000	8.33				
						10.00				
					Tot.	99.83	(2 CPUs)			

Assumptions:		
Digital masking, windowing and frames cropping are performed at WFEEs level		
CPU clock	60	MHz
FPGA clock	80	MHz
Clock cycles/elementary operation	3	
Masking factor (only for VNIR)	0.7	
CPU pipeline stages	5	not used
Available lossless compression factor (spectroscopy)	2.5 max	
VNIR uses the UTR-MULTIACC-mode		
bit/px	16	
No. Science channels	5	
No bits/register	32	not used
Phase A margin (CPU resource occupation)	0.5	50%

Tab. 6 – Extract from the spreadsheet used for ICU on-board processing and data rates/volume evaluation. Bright targets case (most demanding one in terms of processing power). For bright mode ICU sends to ground the evaluated ramp slopes plus a goodness of fit (2 byte/ramp).

The above evaluation has to be considered as preliminary, and a series of performance tests of the baseline processors are planned, based on the use of a LEON3 development board in a laboratory test environment in which two programs modules linked via standard TCP/IP socket in a server-client configuration are used:

- The *Spacecraft simulator program ScSim* (server), which communicate with the ICU via a Space-Wire I/F and with the DPU EGSE via a TCP/IP socket. This program manages the Space-Wire communication protocol by means of a *PCI SpaceWire board from SkyLab.*
- The *DPU EGSE DpuEgse* (client) sends telecommands and receives telemetry to/from the ICU (LEON Board in the test environment) via ScSim. The program sends predefined telecommands sets and receives (display and store) the ICU telemetry by means of a script-like interpreted sequence of commands.

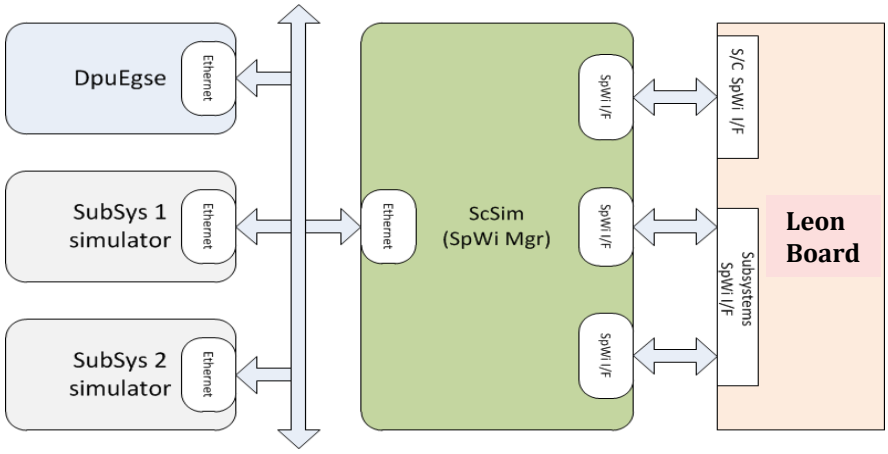

Fig. 26 - Leon Processor Performance Evaluation Test Environment

Due to the TCP/IP socket, the two programs may run on different network connected computers. Another advantage of the server-client architecture is that other clients can connect to the ScSim (which acts as a SpaceWire manager) using one of the four SpW nodes of the SkyLab board, so that it is possible to simulate also other ICU SpW connected subsystems in the EChO payload.

4.5 INSTRUMENT OPERATION MODES

Instrument Operations shall be defined in terms of clearly identifiable operating modes. An operational mode represents an operationally well defined and, within certain limitations, a stable configuration as concerns mechanical, thermal, electrical and functional conditions.

A distinct logical operating mode shall be defined if any of the following conditions apply to the instrument actual mode of operation (EIDA-R-2950):

- Mode results in a significant change in demand on spacecraft resources (e.g. power; data rate);
- Mode requires a specific spacecraft operational status (e.g. thermal environment; pointing; specific DMS functions);
- Mode results in a functionally distinct operating mode of the unit (e.g. calibration function; standby; software maintenance).

The list of the instrument operation modes is reported following the state transition diagram on Figure 27.

OFF mode

All instrument subsystems are off (including ICU and there will be not instrument telemetry). The instrument is unpowered.

Initialize (INIT) mode (TBC)

This is an intermediate mode between OFF and STANDBY. This will be the mode the instrument enters after a power cycle or reboot. This mode refers to two different phases of the switch-on procedure:

- Phase 1 - PROM boot procedure running:
  - Event reports can be generated;
  - In this mode only a limited sub-set of commands may be executed.
  This mode allows updates of ICU on-board SW and/or tables to be carried out safely before they are used for instrument control.

- Phase 2 - The Application software (ICU OBS) is copied from EEPROM to RAM and started.
  The ICU is fully operational; OBS is ready to accept commands from the S/C. Only ICU housekeeping parameters are generated. In this phase the complete start up procedure is performed, switching on one after the other all spectrometers, checking their health by monitoring the housekeeping data.
  When the payload is ON and ready, then the system can transit to the standby mode.

This mode can also be entered autonomously from the SAFE mode and from the STANDBY mode upon reception of a dedicated ICU Reset Command.

STANDBY mode
In the standby mode the following assumptions are made:

- The S/C may be pointed in any arbitrary direction;
- Housekeeping Telemetry packets only will be provided.

No science data is transmitted and therefore the instruments will not fully use the available telemetry bandwidth.
ICU and FPAs are operational.
The mechanisms (if present) are initialized and set to their home position.
This mode will be used when the scientific payload is not being used for observations for an extended period of time.

SAFE mode
This mode shall always be automatically entered when an instrument or a system failure case occurs; through the failure detection, isolation and reconfiguration (FDIR) process the instrument shall be able to survive in this mode indefinite time before ground intervention has to occur.

CONFIGURE mode
In this mode the overall scientific payload is configured for the execution of the next observations.
- The S/C is pointed to the target sources.
It is not possible a direct transition to science mode from Standby without a step in the configuration mode.

SCIENCE mode(s)
In the Science modes the following assumptions are made:

- the S/C is pointed to the target sources;

- the spectrometers are active and configured.

All Subsystems are fully operational. The science mode is the one of the payload performing scientific observations.

DIAGNOSTIC mode
This mode is entered for testing purposes. It is an extended science mode that can be used on ground for instrument calibration and on flight for instrument maintenance.

MEMORY MANAGEMENT mode
This mode is entered for on board memory management (memory load, dump and check) activities. This mode can also be entered also in case of memory (both PM and DM) patching at runtime.

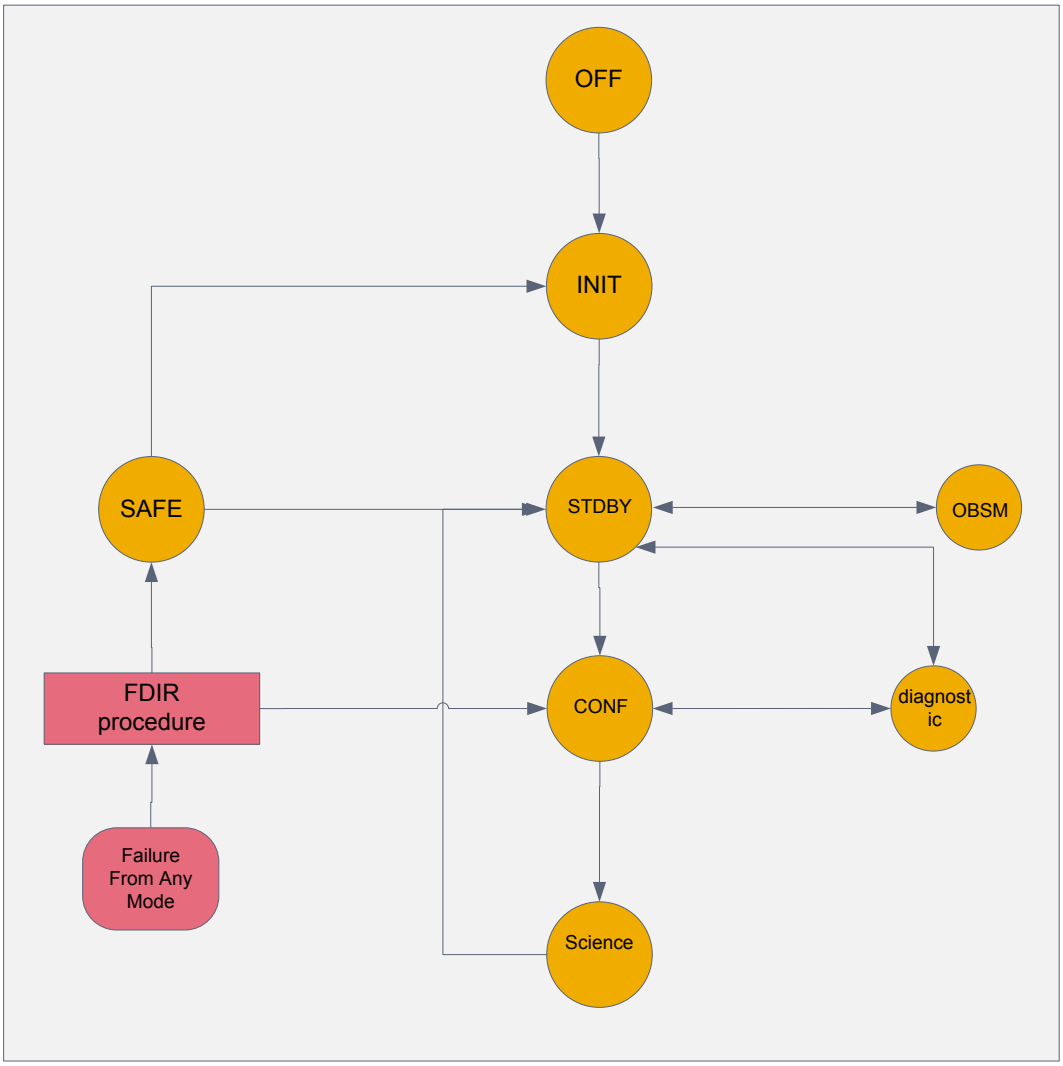

Fig. 27 – State transition diagram of instrument operation modes.

5 CONCLUSIONS AND FUTURE DEVELOPMENTS

The Assessment Phase EChO Payload electrical architecture has been defined and described by means of this Technical Note. Some still open issues as e.g. the overall processing capabilities depending mainly from the adopted on board deglitching procedures (TBC/TBD) and data volume/data rates to be fulfilled as well as the use of the MIL 1553 for the FGS and its overall I/Fs configuration w.r.t. ICU and/or platform shall be addressed by further analysis taking into account the Consortium responsibility and design philosophy from a side and the system efficiency and reliability from the other side as driven by the ESA and Prime Contractor documentation.

Future developments during the next phase (Phase B) will consider these issues from the different perspective of the Definition Phase design.

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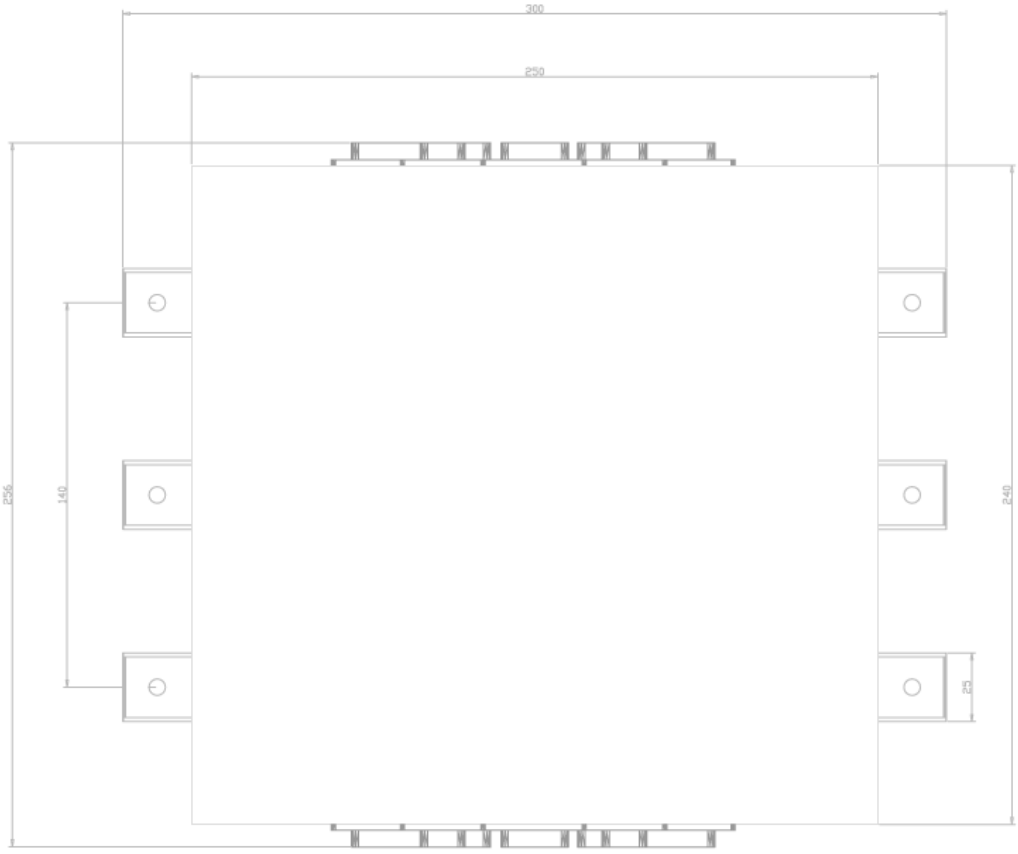
7 ACKNOWLEDGMENT

We acknowledge the financial contribution by the *Italian Space Agency* in the framework of the ASI-INAF agreement I/022/12/0.

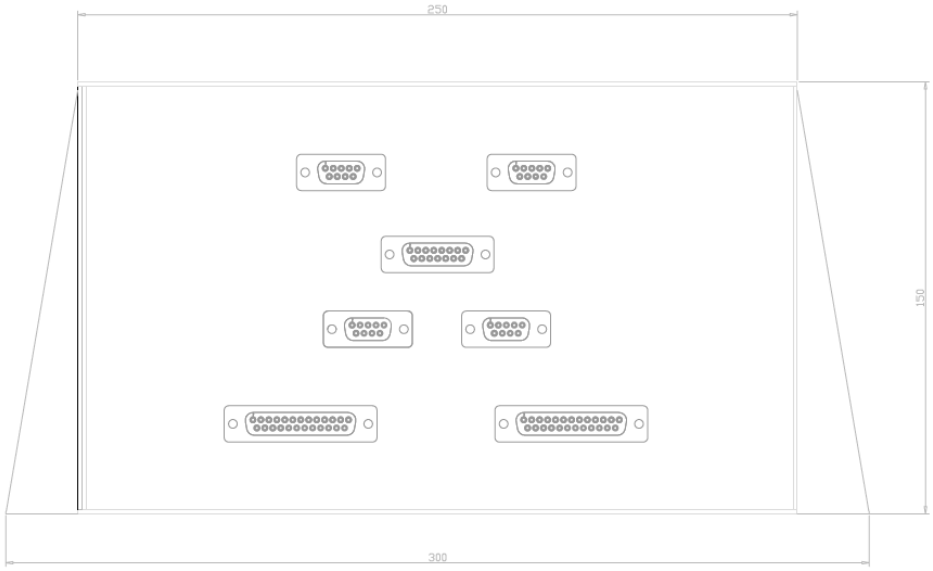
8 APPENDIX A

Appendix A contains the ICU and WFEEs boxes Mechanical Interfaces Control Drawings (MICDs).

8.1 ICU BOX MICDS

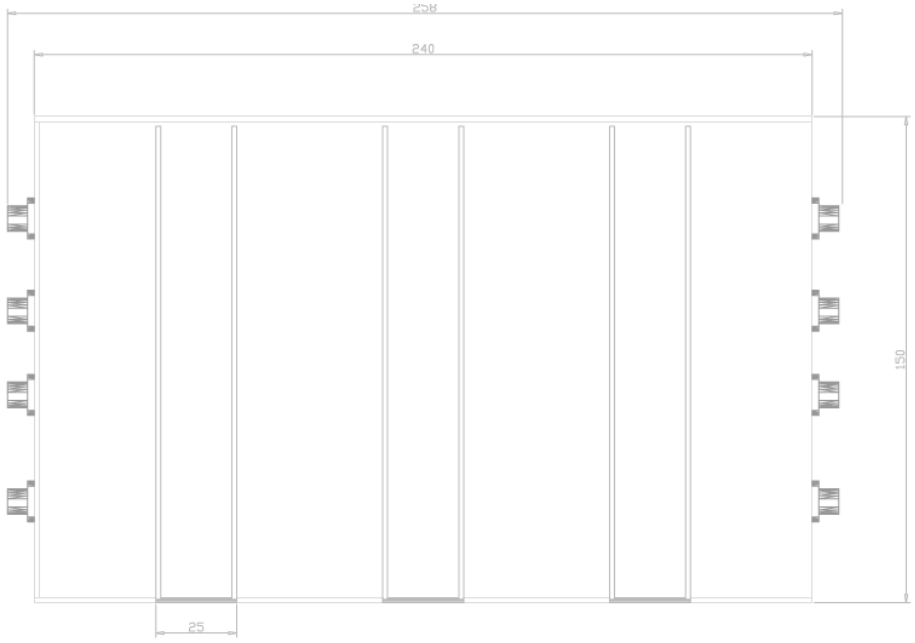


ICU TOP VIEW MICD



ICU FRONT VIEW MICD

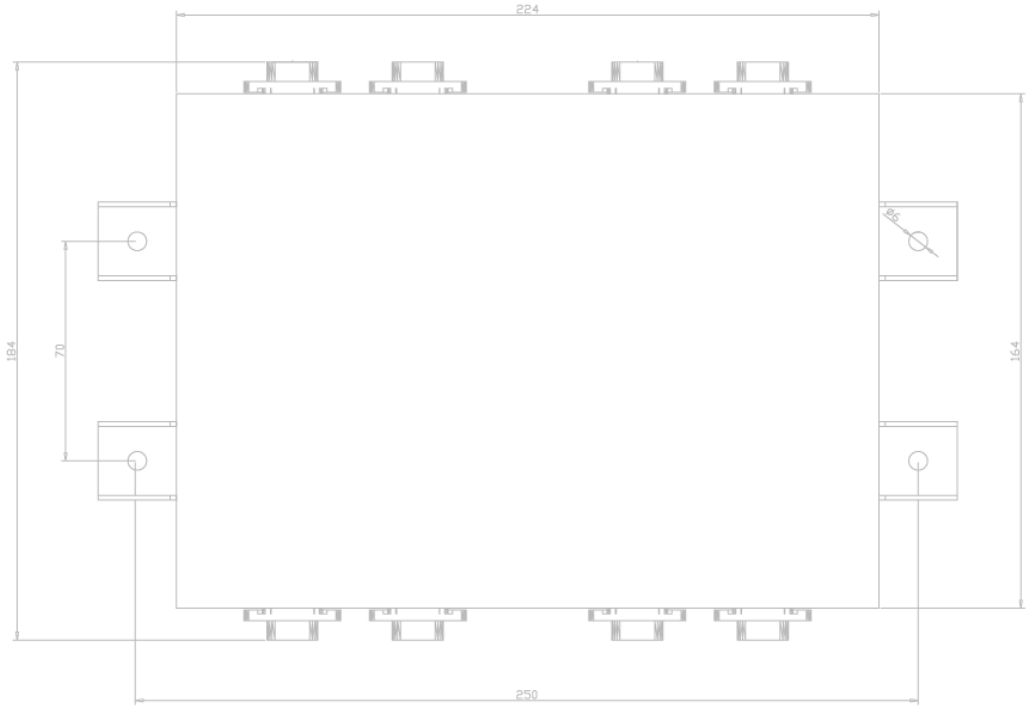
(connectors # and location are TBD/TBC and for illustration purpose only)



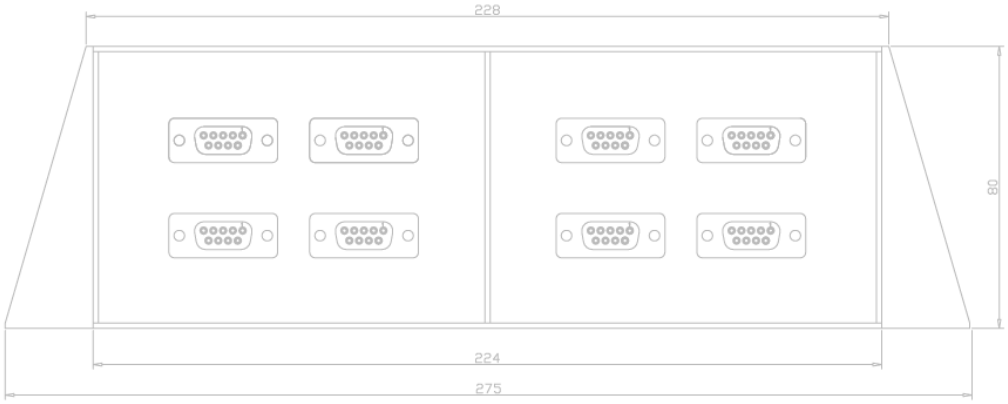
ICU SIDE VIEW MICD

(connectors # and location are TBD/TBC and for illustration purpose only)

8.2 WFEEs BOX MICDs

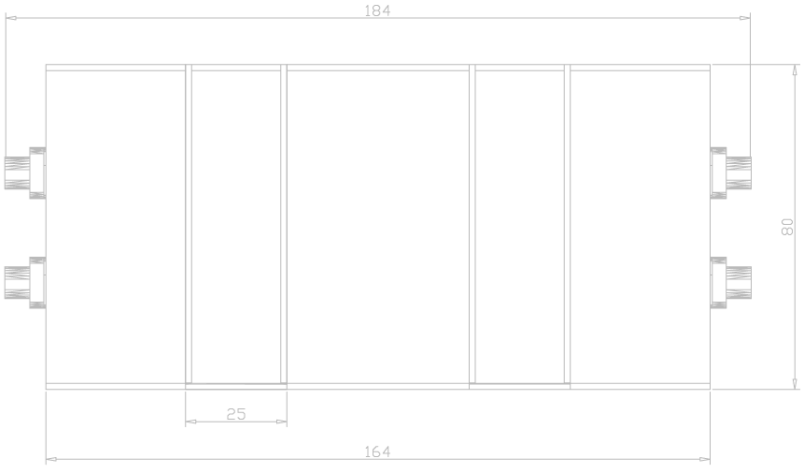


WFEEs TOP VIEW MICD



WFEEs FRONT VIEW MICD

(connectors # and location are TBD/TBC and for illustration purpose only)



WFEEs SIDE VIEW MICD

(connectors # and location are TBD/TBC and for illustration purpose only)