16-Bit Sigma-Delta Analogue-to-Digital Converter

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IWF Space Research Institute

Fraunhofer Institut Integrierte Schaltungen

Overview

- Design drivers
- Involved institutes
- ASIC design (magnetic field and voltage mode)
- Performance
- Radiation tests
- Conclusion and outlook

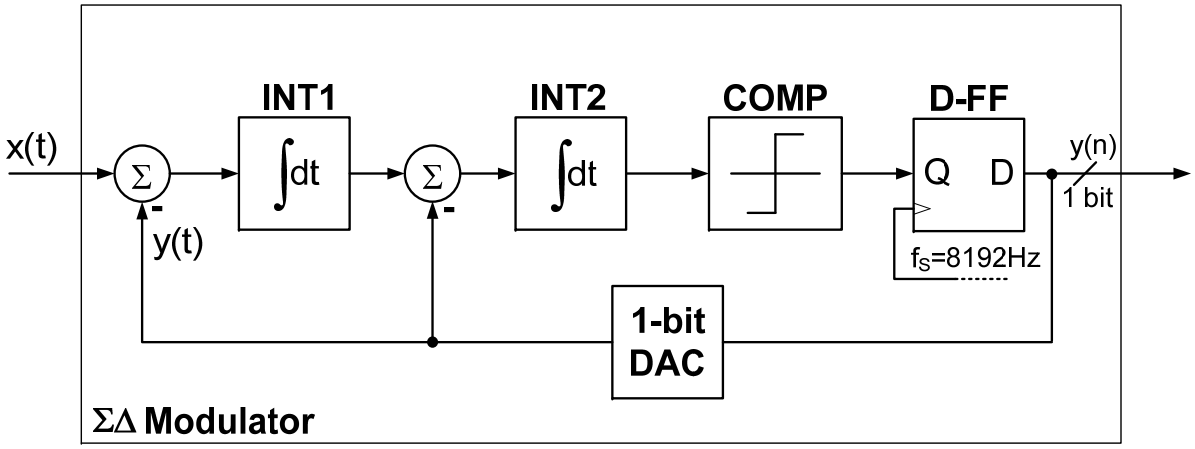
Design Drivers

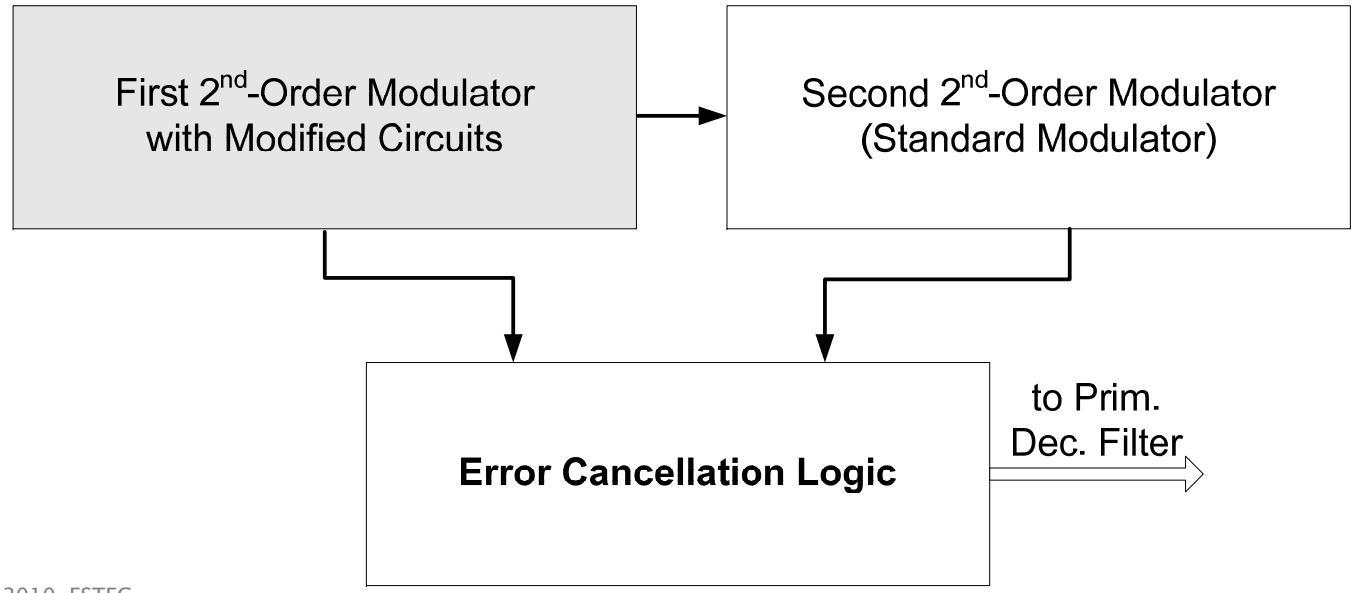
- Miniaturization
- One ASIC for magnetic field and voltage ADC applications
- 16-bit performance, 100Hz sample rate
- Low power
- Suitability of 0.35µm mixed-signal CMOS process from austriamicrosystems (multi project waver)
- Radiation hardness was no design driver!

IWF and Fraunhofer IIS

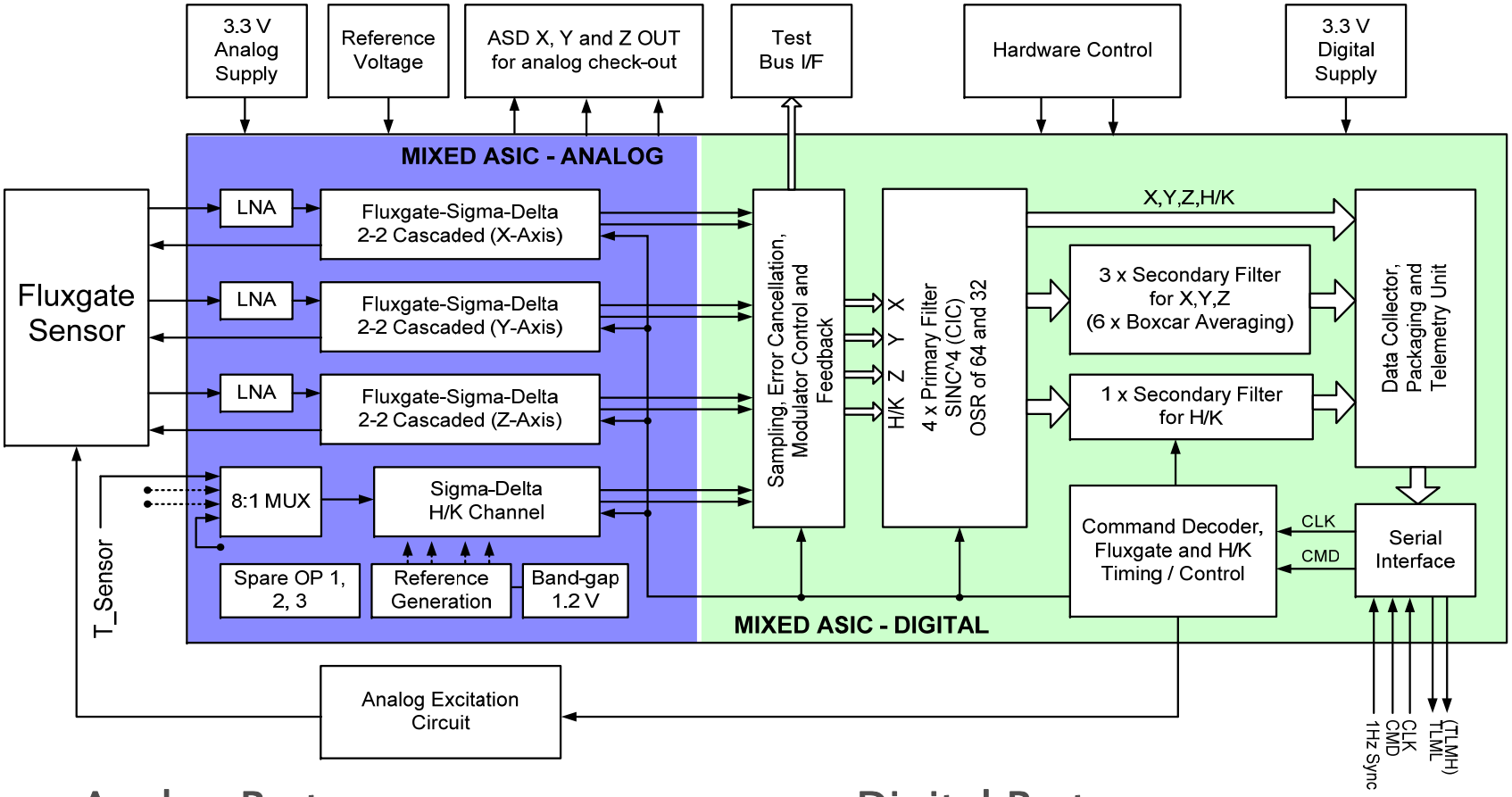
- Space Research Institute (IWF) of AAS in Graz, Austria
  - Development of fluxgate magnetometers, satellite potential control units, atomic force microscope, electron drift instrument ...
  - Involved in Cluster, Rosetta, BepiColombo, MMS, etc.
- Fraunhofer Institute for Integrated Circuits in Erlangen, Germany
  - One of the largest institutes within the Fraunhofer organization
  - Develops integrated circuits, electronic equipment and complex systems

2-2 Cascaded Sigma-Delta



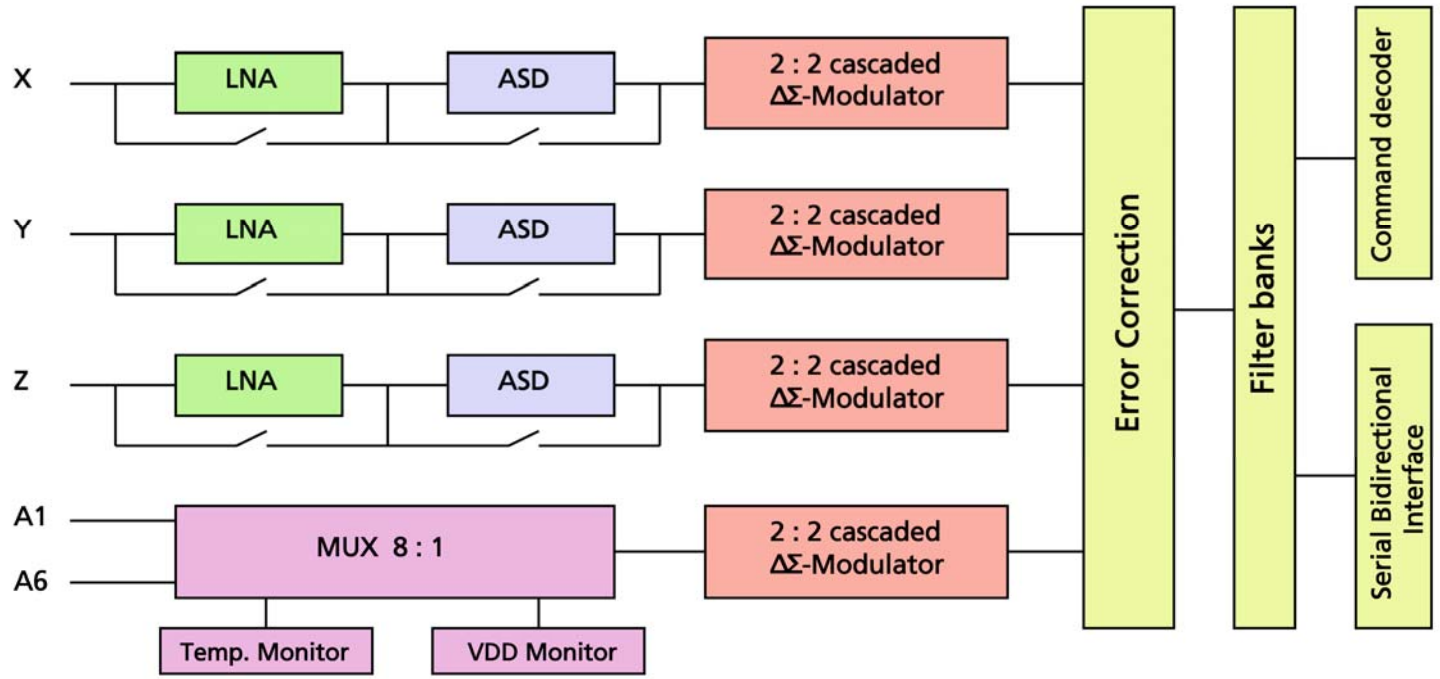


Block Diagram Field Mode



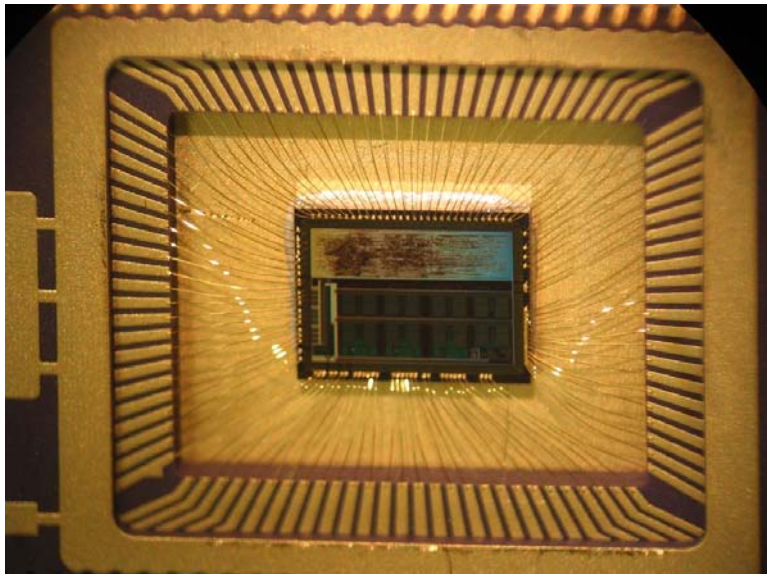
- Analog Part:
  - 3 fluxgate channels with LNA
  - 1 housekeeping channel w/mux.
  - Reference generation
  - 4 spare op-amps
- Digital Part:
  - Primary and sec. decimation filter
  - 4-wire serial synchronous I/F
  - Command decoder, Clk-generation
  - Test bus interface

General Purpose ADC

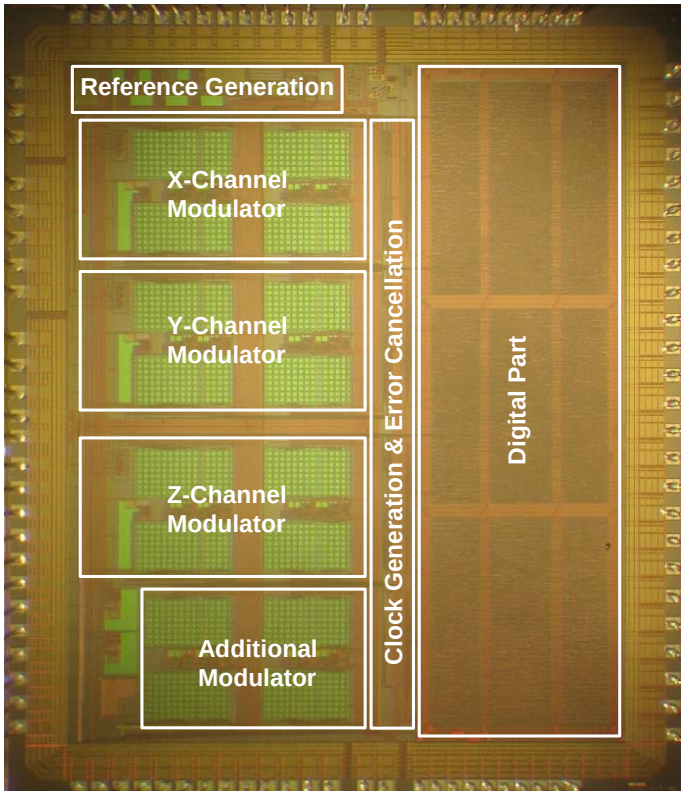


- 4- to 11-channel general purpose ADC
- Configuration A:
  - 4 channels with 128 Hz data rate
  - X, Y, Z and HK (A1) with ±1.25V
- Configuration B:
  - 3 channels with 128 Hz data rate
  - 1 channel with 2 Hz and ±1.25 V; 5 channels with 2 Hz and ±0.625 V
  - 2 additional channels measure supply voltage and MFA temp. with 2 Hz

Package and Chip Monograph

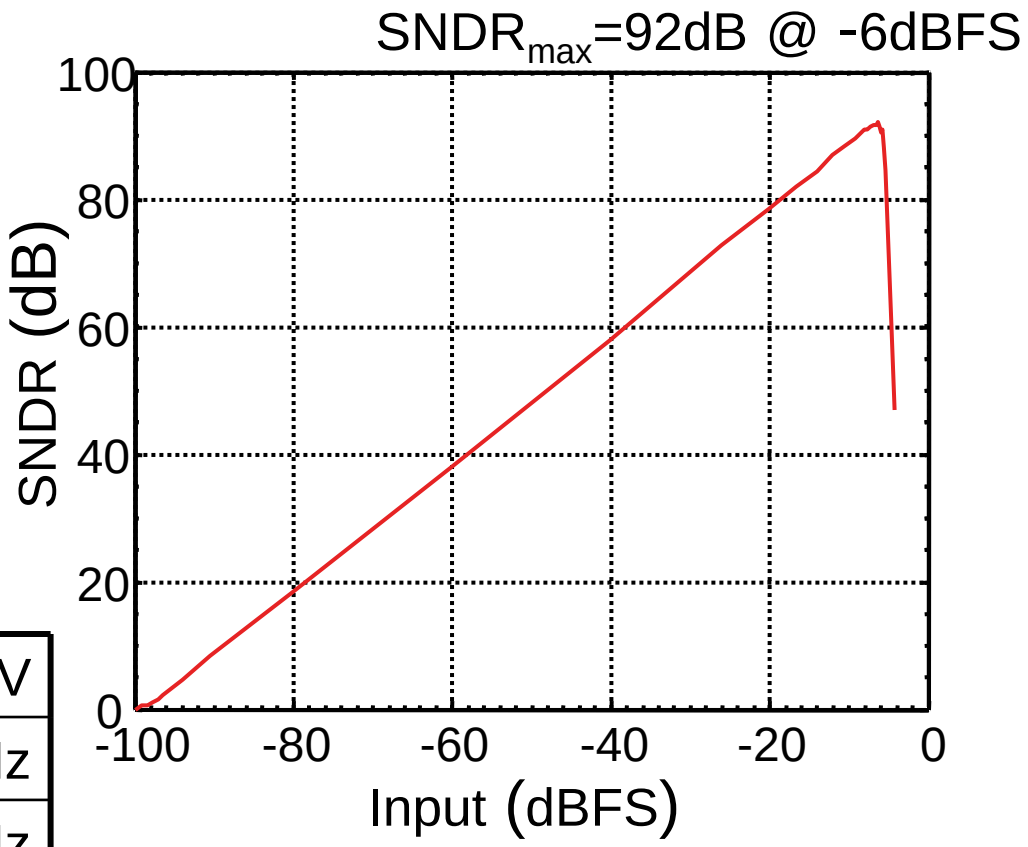


Die bonded to 100-pin CQFP package



Chip micrograph (ca. 20 mm^2)

Signal to Noise and Distortion Ratio

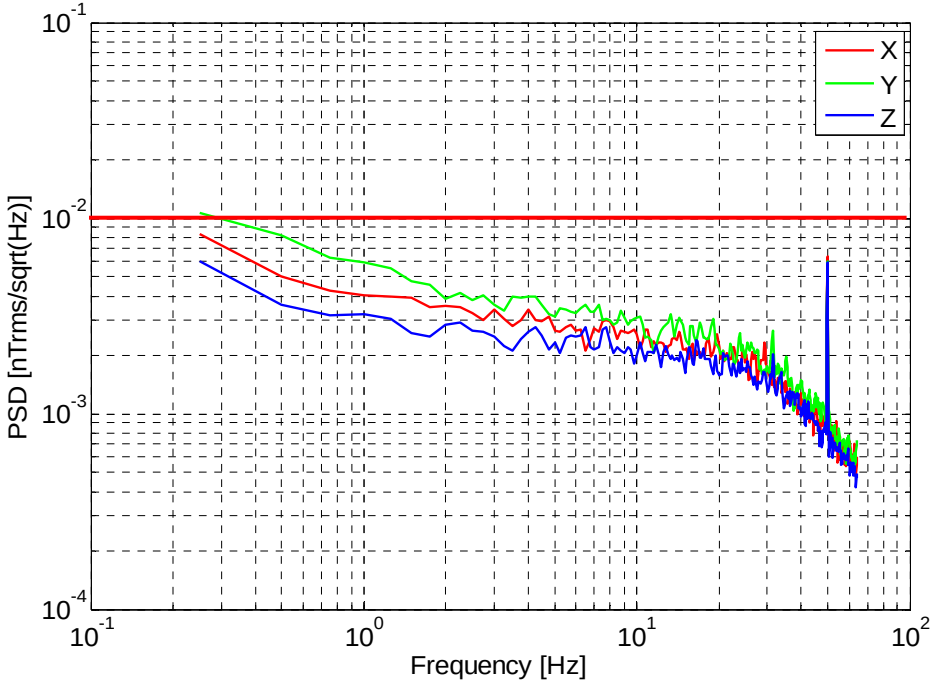


Fullscale	±1.25V
Clock Rate	8.192kHz
Output Rate	128Hz
OSR	64
DR	98dB
SNDR$_{max}$	92dB

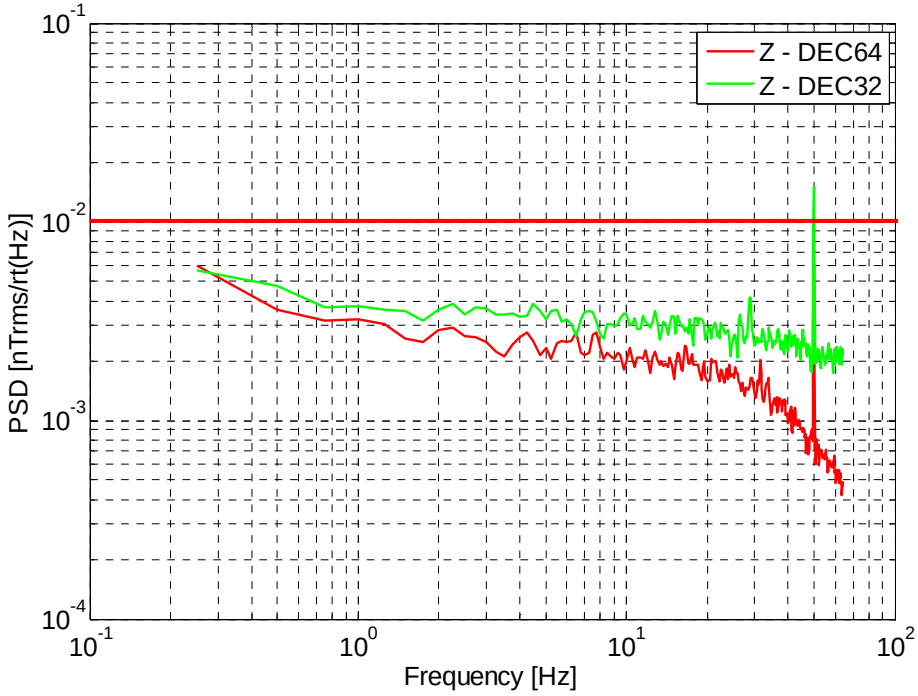
Noise Level in Field Mode

Engineering Model for MMS with fluxgate sensor from UCLA

X, Y and Z in DEC64



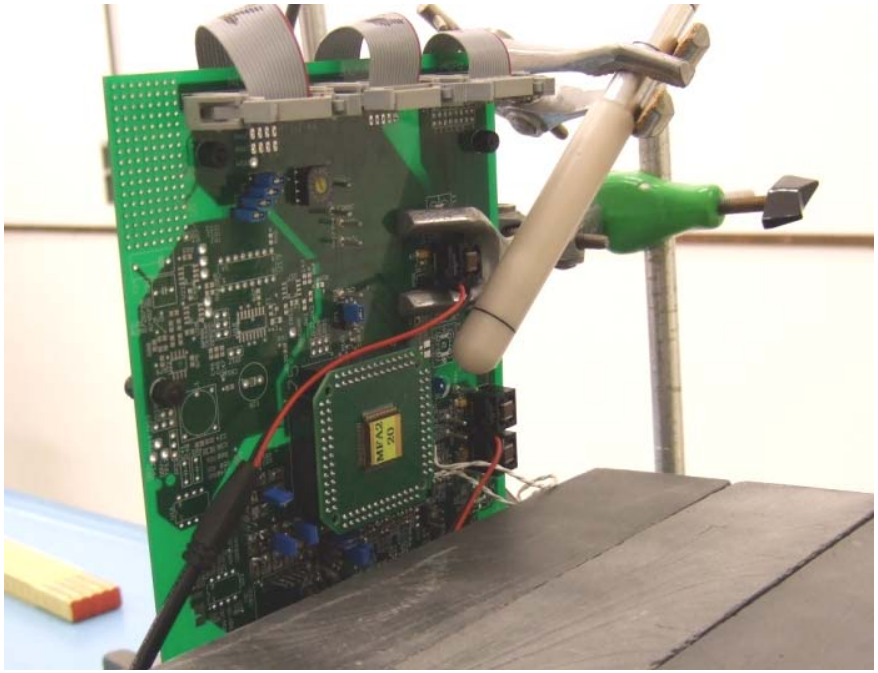
Comparison of Z in DEC32 and DEC64



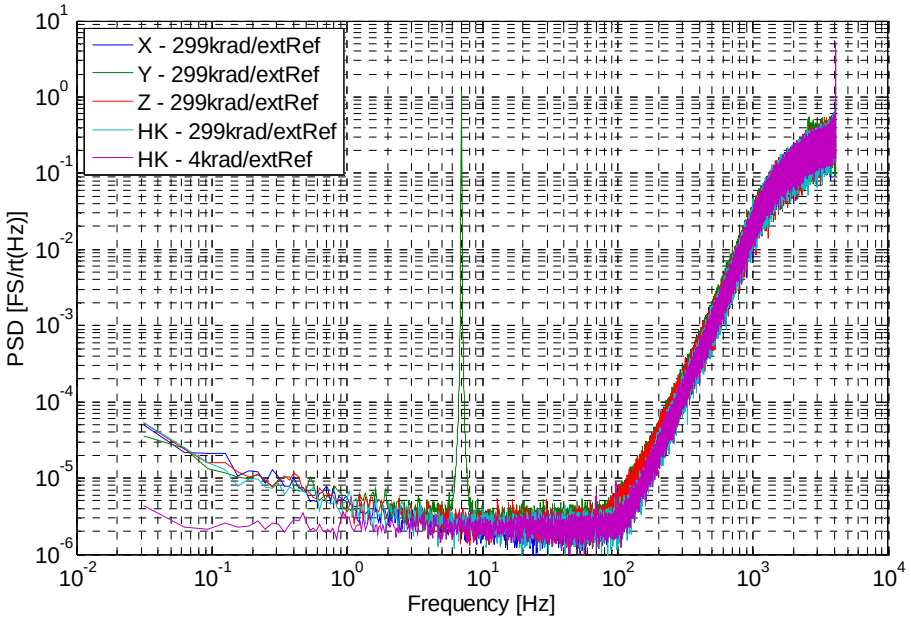
- All three components well below the standard requirement for a fluxgate magnetometer (red line)
- Noise floor in 60Hz bandwidth mode (Z – DEC32) is little higher than for the 30Hz mode (Z – DEC64)

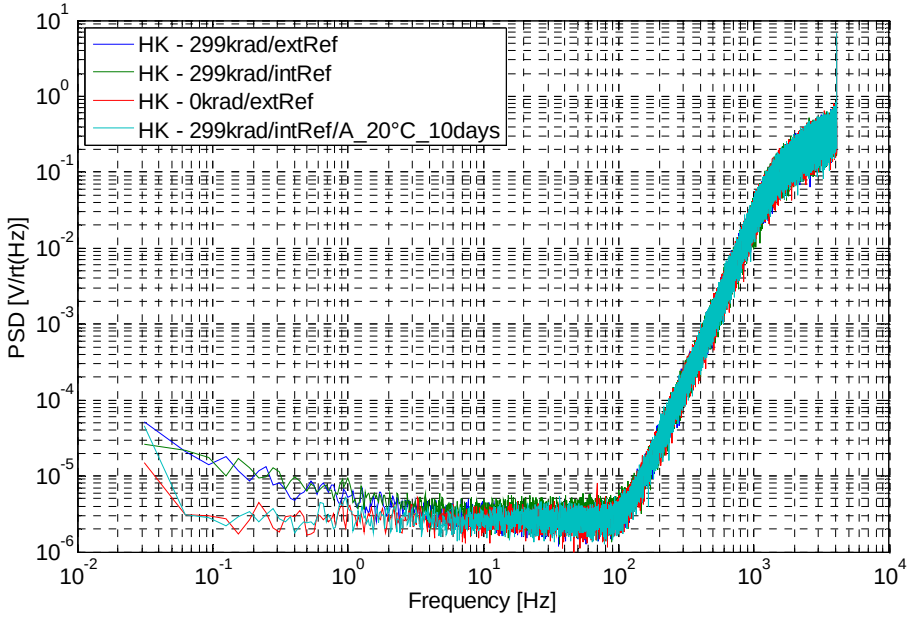
Radiation Tests

- TID test 1
  - 2-2 cascaded modulator from Fraunhofer IIS
  - Up to 115 krad
- TID test 2 (MFA-1)
  - Functional up to 260 krad
  - Linear drop of SNDR (0.04 dB/krad)
- TID test 3 (MFA-2)
  - Functional up to 300 krad
  - 1/f noise above 130 krad
- SEE test 1 (MFA-1)
  - SEL LET_{TH} of 14.1 MeV*cm²/mg
  - σ_{SAT} of 10^{-3} cm²/device
- SEE test 2 (MFA-3)
  - See below



TID Test with MFA-2 (@ ESTEC)

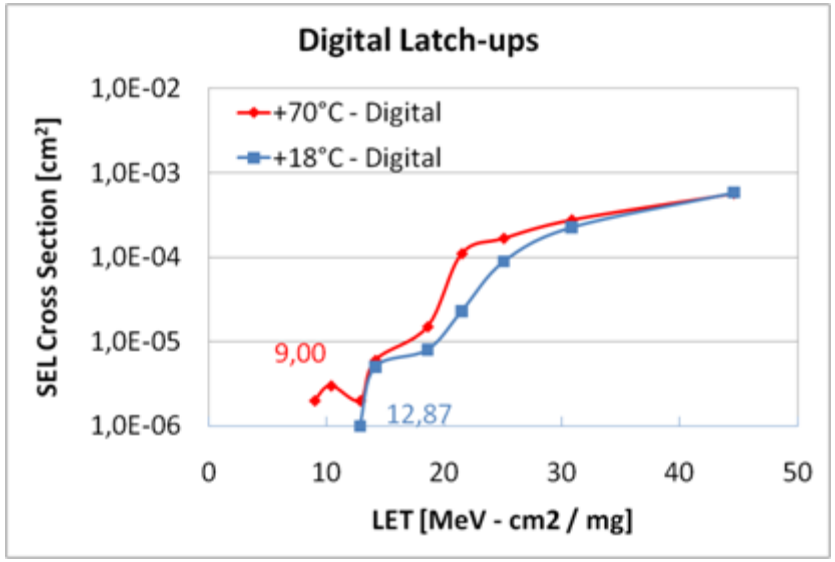




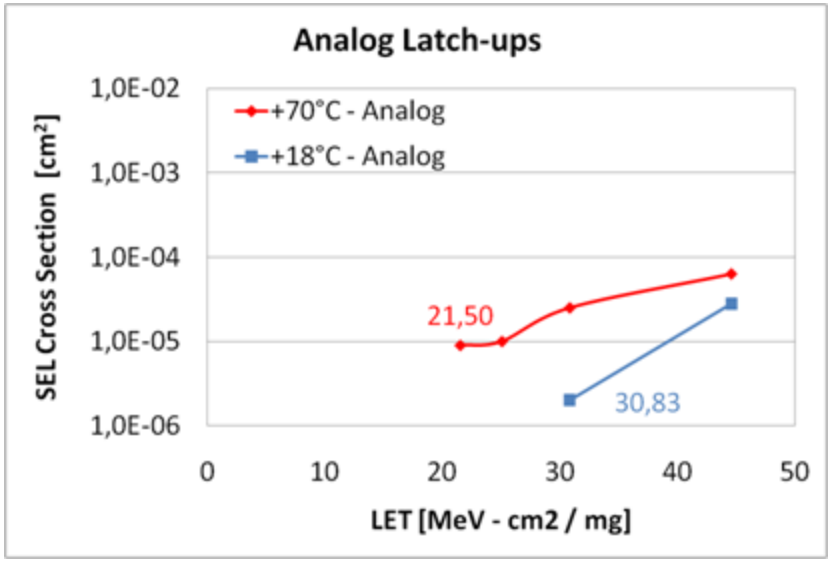
- Fully functional up to 299krad
- Test board was configured in external voltage mode
  - Fluxgate channels with different ranges and set-ups
- Increase of 1/f-noise with TID above 170krad
- All four channels show same behaviour
- No difference between internal and external voltage reference
- Increased noise disappears after 10 day annealing at room temp.

SEE Test 2 with MFA-3 (@ TAMU)

Digital Latch-up



Analog Latch-up



- Linear Energy Transfer Threshold (LETth):
  - Digital: LET_{th} (+18°C) = 12.9 MeV-cm²/mg; LET_{th} (+70°C) = 9 MeV-cm²/mg;
  - Analog: LET_{th} (+18°C) = 30.8 MeV-cm²/mg; LET_{th} (+70°C) = 21.5 MeV-cm²/mg;
- Saturation Cross Section (σ_{SAT})
  - Digital: $\sigma_{SAT} = 10^{-3}$ cm²
  - Analog: $\sigma_{SAT} = 10^{-4}$ cm²

Summary Tables

MFA Summary

Process:	CMOS 0.35 µm
Fabrication:	austriamicrosystems
Layers:	2 poly, 4 metal
Chip area:	20 mm²
Package:	CQFP-100
Gate equivalent (digital):	25,000
Transistors (analog):	14,000
Delta-sigma modulators:	Three fluxgate, one housekeeping
Digital interface:	4-wire serial synchronous
Synchronization:	Per command

MFA Resource Requirements

Supply voltage:	3.3 V digital 3.3 V analog
Power consumption:	10 mW digital 50 mW analog 60 mW total
PCB area:	< 9x6 cm^2
Data interface:	TLMH channel: 128 Hz TLML channel: 2-128Hz

MFA Performance Characteristics

Total dose hardness:	Full specs: 170 krad Functional : > 300 krad
Single event latch-up:	> 13MeV•cm^2mg^{-1}
Dynamic range (field):	< ±60,000 nT; 92 dB
Dynamic range (voltage):	± 1.25 V (differential) ± 0.625 V (single-ended)
Digital resolution:	23 Bits
SNDR (field):	85 dB
SNDR (voltage):	92 dB (bandwidth: 30Hz)
Offset stability (field)	< 10 pT/°C MFA temperature < 0.4 nT/250h
Gain stability (field)	50 ppm/°C (± 2,000 nT range)

Conclusion and Outlook

- MFA-3 is close to full qualification for NASA's MMS mission
  - Life test is ongoing; screening and qualification will be finished with DPA in Feb. 2010
- MFA-3 could be used for JGO mission as is
  - but latch-up protection is required for the 3.3V supply
  - ASIC is very robust in case of a latch-up (non destructive)
- It is considered to make future MFA designs fully radiation hard by
  - either developing a rad-hard digital library for the currently used C35 process from austriamicrosystems
  - or to transfer the current design to a process with an existing rad-hard, digital library (e.g. UMC 0.18 µm) in the upcoming years.
- IWF/Fraunhofer IIS team would like to participate in *AO/1-6346/09/NL/AF – Radiation tolerant analogue/mixed signal technology survey and test vehicle design* as subcontractor