Issues in (very) rad hard systems: an ESA perspective on use of COTS and space grade electronics in JUICE mission.

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Darmstadt – 9-11 November 2011

European Space Agency

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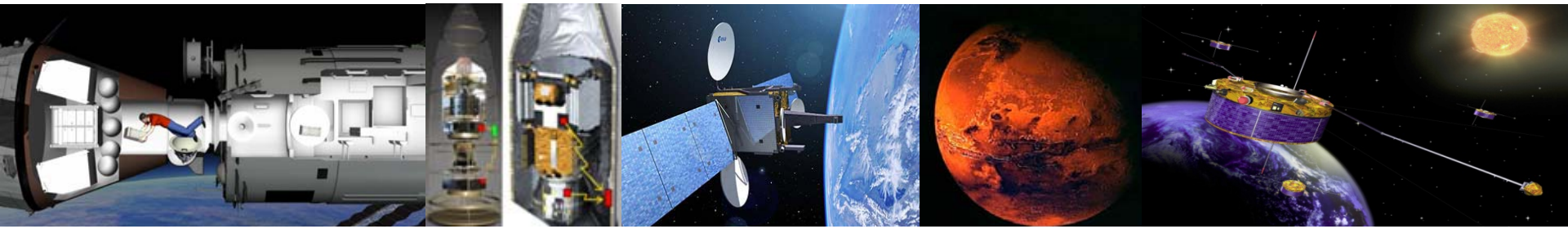
Short Summary

- Future Reference Scenarios and additional considerations for On Board Computers, Data Handling and Data Systems,
- Technology Trends,
- Building Blocks,
- Designing with FPGAs, opinions and lessons learnt
- The special case of memories
    - How to protect ‘soft’ COTS memories
- ESA Developments of interest for JUICE instruments

Future Reference Scenarios

Future programs for **Science, Exploration, Earth Observation and Telecom** are the sources of high demanding requirements for the next generation of on-Board Avionic Systems:

- **increase of processing capabilities,**
- **reduction of mass, volume and power,**
- **implementation of functional services linked to on-board communication**,
- **rationalization of interfaces,**
- **new architectures for lower level and application SW,**
- **enhanced modularity and multi-instruments support capability (Science),**
- **high data throughput links and increased memory capacity (Science & Earth Obs.)**



Future Reference Scenarios

Recent advances made in the field of Time and Space partitioning benefiting from sophisticated memory management functions implemented in CPUs must be supported as well.

The increasing request of higher performance in term of MIPS/MFLOPS calls for the increase of the clock frequency of mono-core solutions and/or development of multi-core (homogeneous or heterogeneous) processors following a well consolidated trend that has started several years ago in the commercial/embedded markets. Clearly the operative system(s) and the SW development/implementation tools have to be accordingly improved.

As alternative or also as complementary solution distributed processing power architectures calls for the development of uControllers that can offload the main processor from defined tasks.

Finally the use of COTS components has to be positively considered as alternate solutions where the existing space qualified devices are not able to provide the required performances

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Technology Trend: On-Board Computers & Data systems Architectures

Space industry and Agencies have recognized the increasing need to raise the level of standardisation in spacecraft avionics systems in order to

- ❑ increase efficiency,
- ❑ reduce development cost and schedule,
- ❑ and operate in more optimized development and verification environment.

How to reach these goals ?

- ❑ **Rationalisation of Data Systems and OBC architectures**,
- ❑ Definition of **Generic specifications for OBC and RTU**
- ❑ Implementations of **building blocks** approach to allow easy re-use of sub-elements,
- ❑ Introduction of **new technologies** as Point-of-Load Converter (PoL), Multicore processors , NoC, very high speed interfaces (Inter-processor interface, SpF,...) ...

Technology Trend: System on a Chip

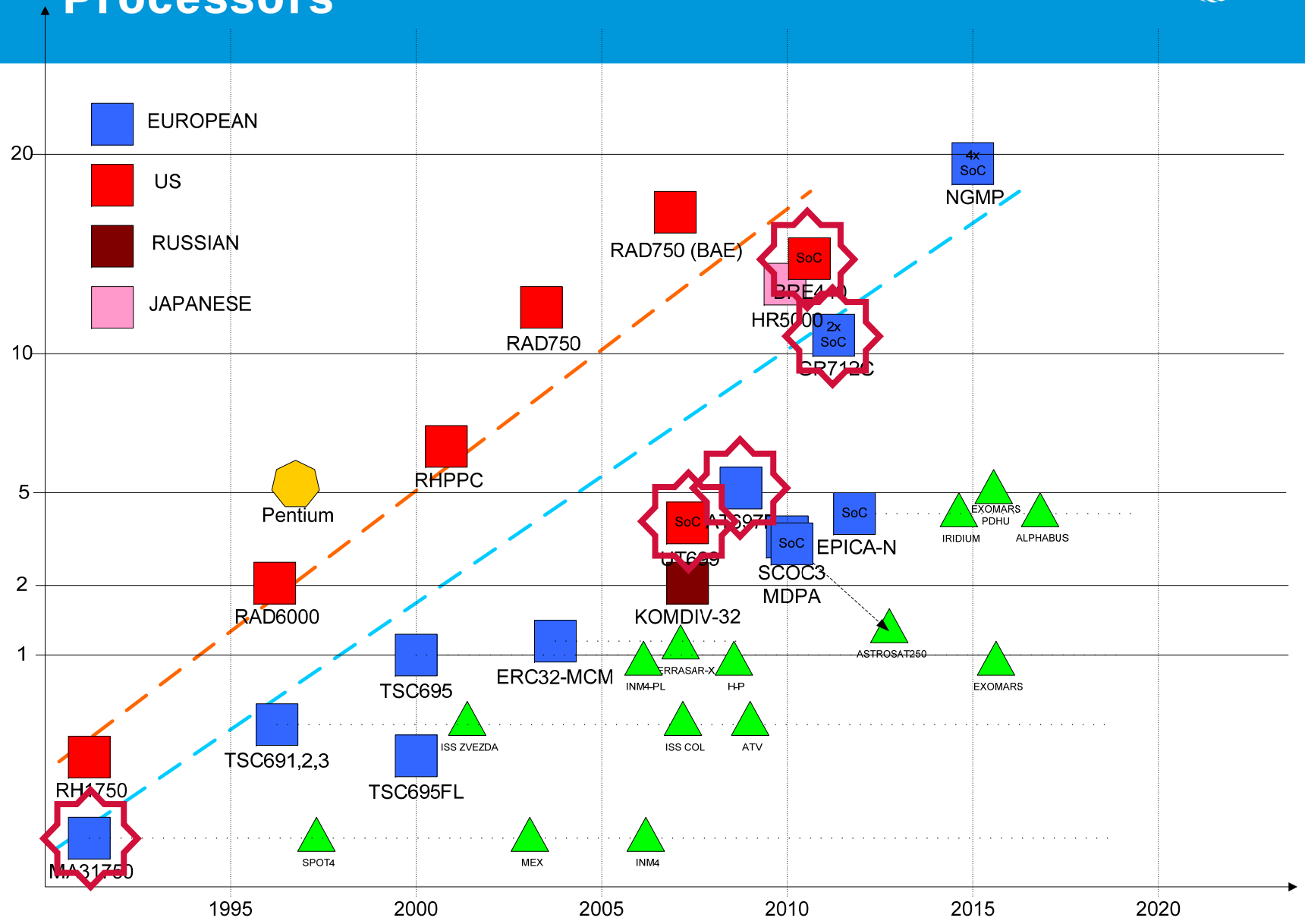
System-on-a-chip solutions where the typical functionalities of a microprocessor are integrated with other SMU/OBC/CDMU functionalities (like CCSDS TM/TC interface or external interfaces as SpaceWire, MIL-STD-1553B, CAN, Packet Wire and distribution of synchronization signals) have been already developed using in Europe using different .18 ASIC technologies:

- **SCOC 3** (developed by Astrium-F - ATMEL)
- **MDPA** (developed by Astrium-D - ATMEL)
- **COLE** (developed by RUAG-S - ATMEL)
- **EPICA-NEXT** (under development by TAS-I - ATMEL)
- **GR712RC** (developed by Aeroflex Gaisler - TOWER)

And all these SoC products will shortly fly:

- SCOC3 on **Seosat** as main core of the Astrium Computer called OSCAR (Optimized Space Computer Architecture with Reconfigurable LEON3) and on Astroterra
- MDPA as P/L controller in **Alphasat**
- COLE as core processor of the **SGEO platform** SMU
- EPICA-NEXT as core processor in the computer of **Iridium Constellation**

Status of General Purpose Space Processors



Technology Trend: System on a Chip

Reduction of power consumption, mass and dimensions achievable with silicon evolution and introduction of the SoC technology are significant and rapid:

GOCE (2009) CDMU
TAS-I *ERC32*

Power consumption = < 90 W average (excluding external loads)
Mass = 21kg
Dimensions = 470(L)x272(H)x332(D) mm

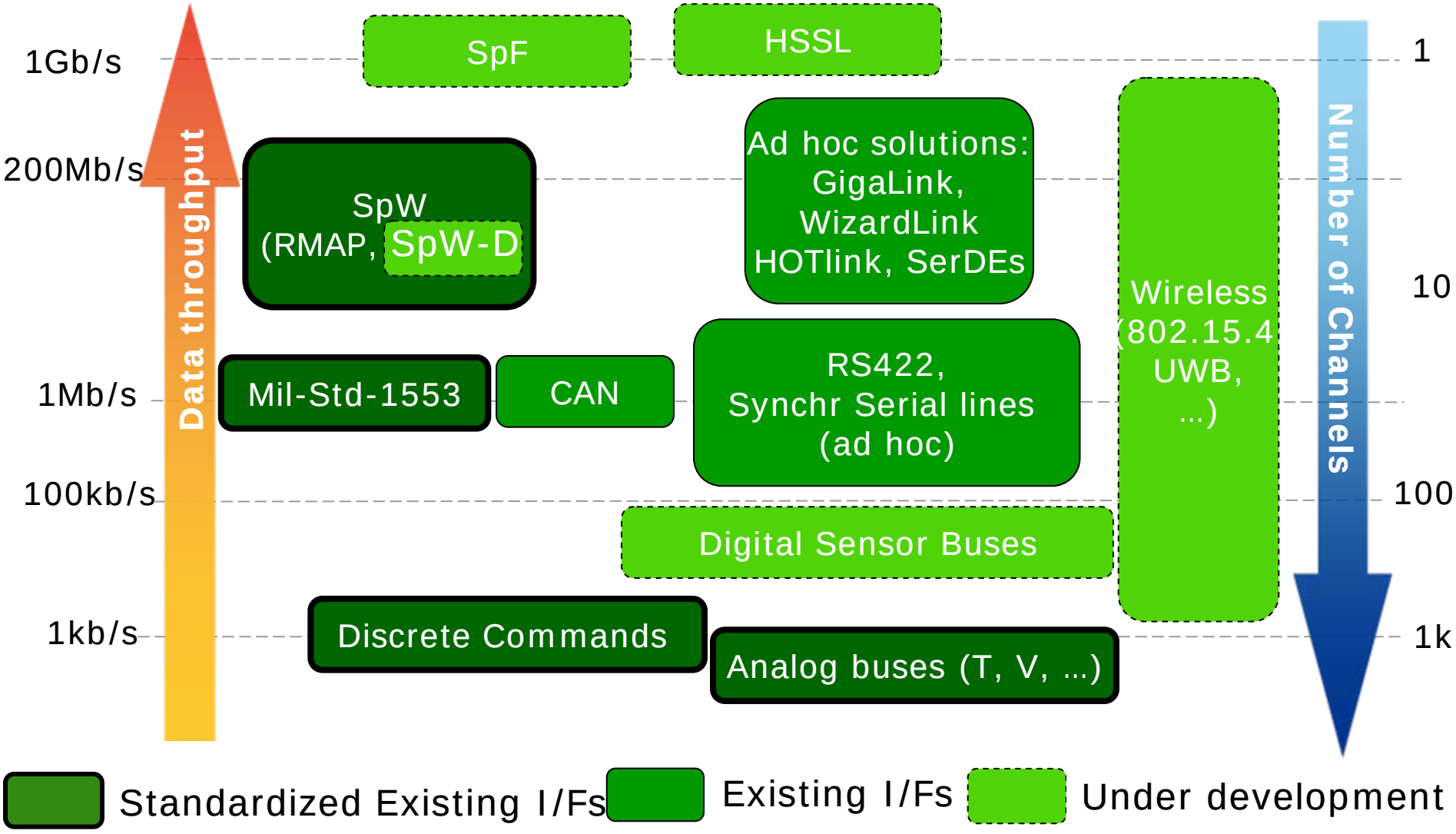
GAIA (2013) CDMU
RUAG-S *AT697*

Power consumption = <40W average (excluding external loads)
Mass = 16kg
Dimensions = 420(L)x270(H)x(276(D) mm

SEOSAT (2014) OBC
ASTRIUM-E *SCOC3*

Power consumption = 15W peak (excluding external loads)
Mass = 5.2kg
Dimensions = 250(L)x150(H)x216(D) mm

Technology Trend: System Busses & I/Fs



Technology Trend: System Busses & I/Fs

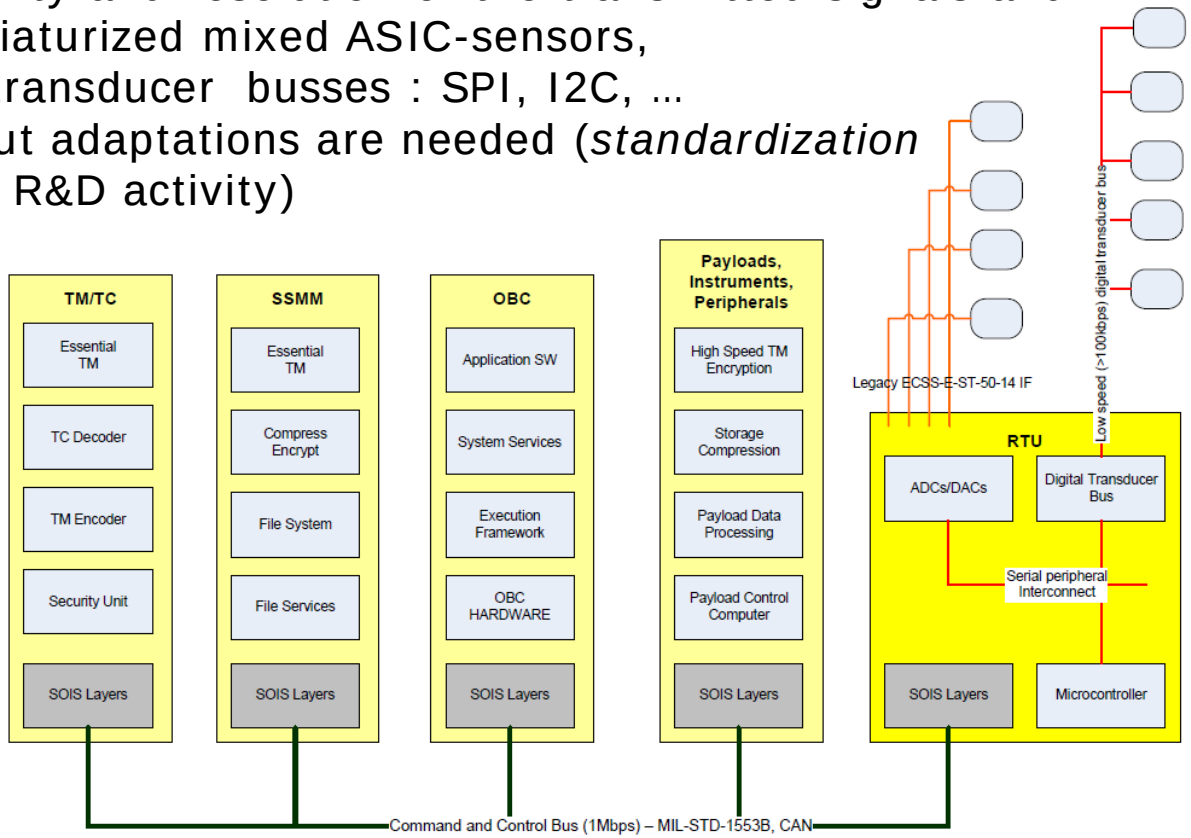
MIL-STD-1553 (1Mbit/s, master-slave multi-point architecture) is used virtually in all ESA and European OBDH systems, and the considerable amount of experience and know-how built by European industries in this field is resulting in a de-facto standard interface for the avionics data systems. **ECSS-E-ST-50-13C**

SpaceWire is a standard for high speed links (<200Mbit/s, point-to-point architecture, LVDS as physical layer) and networks for use onboard spacecraft, developed by the European Space Agencies in collaboration with European Universities and Industries. **ECSS-E-ST-50-12C, ECSS-E-ST-50-5xC**

Controller Area Network **CAN** (1Mbit/s, master-slave multi-point architecture) standard adopts an ISO layering, having the physical (bit) layer well separated from data link and network layers. Nowadays for space applications the CAN bus can use RS-485 as underlying physical layer. **CANOpen** is a higher layer protocol for the embedded world introduced in the 1990s and selected by the as protocol for space missions.
ESA drive a standardization process resulting in recommendations to extend the CAN bus and CANOpen specification to cover aspects that are required to satisfy onboard spacecraft needs (e.g. redundancy). **ECSS-E-ST-50-15 Draft**

Technology Trend: Digital Sensor Busses

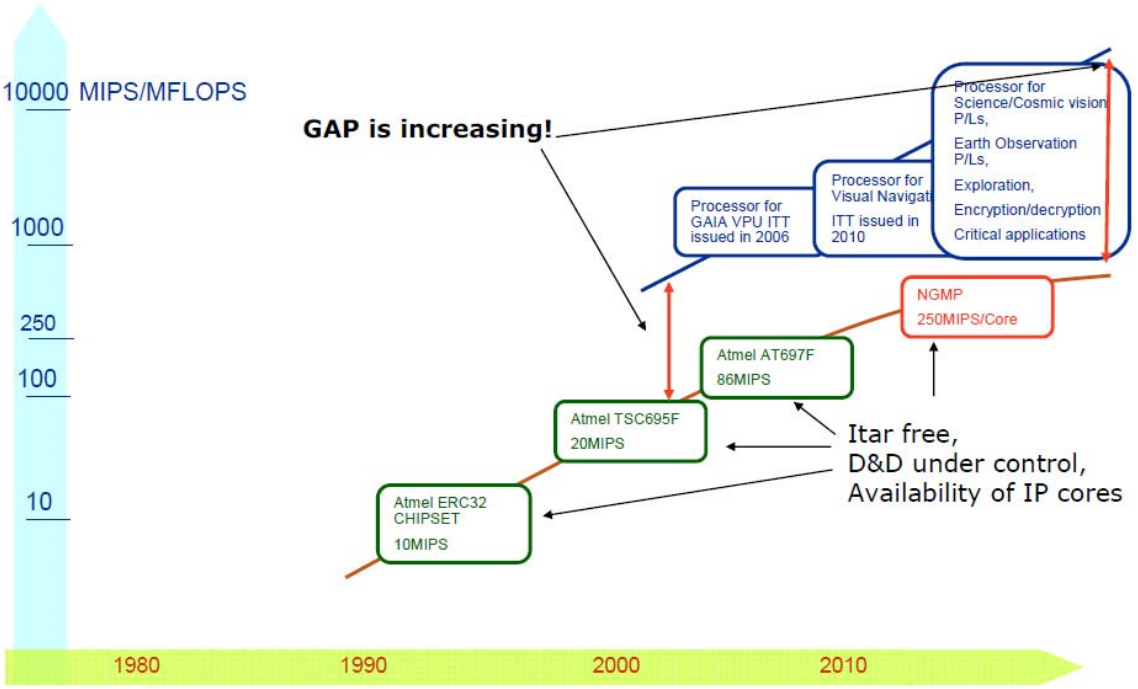
- **ECSS-E-ST-50-14C** defines analogue interfaces, bi-level discrete interface and serial digital interface (16-bit).
- An evolution towards **digital sensor busses** is pushed by the need to increase the signal integrity and resolution of the transmitted signals and by the availability of miniaturized mixed ASIC-sensors,
- candidates for digital transducer busses : SPI, I2C, …
- spin-in technologies but adaptations are needed (*standardization of digital interfaces*- ESA R&D activity)



Technology Trend : COTS Based Computer

- In term of pure processing power capabilities the majority of the mission needs can be served by space qualified products but a small percentage of applications asks for **more performances**, an example is the Video Processing Unit of the GAIA mission,

Note: the usage of commercial components does not mean a cost reduction with respect to a solution that makes exclusively use of fully space qualified products: analyses, specific test (e.g. tolerance against radiation effects) and extra logic are needed.



Technology Trend:
Validation of Reference Architectures

HW Reference Architectures must be validated and the early anticipation of this validation has evident advantages,

Validation can be performed at a full complete SW simulation level or in a mixed configuration HW/SW.

In the Avionics LAB of ESA we have a Reference Architecture System Testbed for Avionics (RASTA).

Its versatile functions and configuration options are intended to be used by network designers, development engineers and test engineers. Its open design and widespread use areas makes it well-suited for dissemination within industry.

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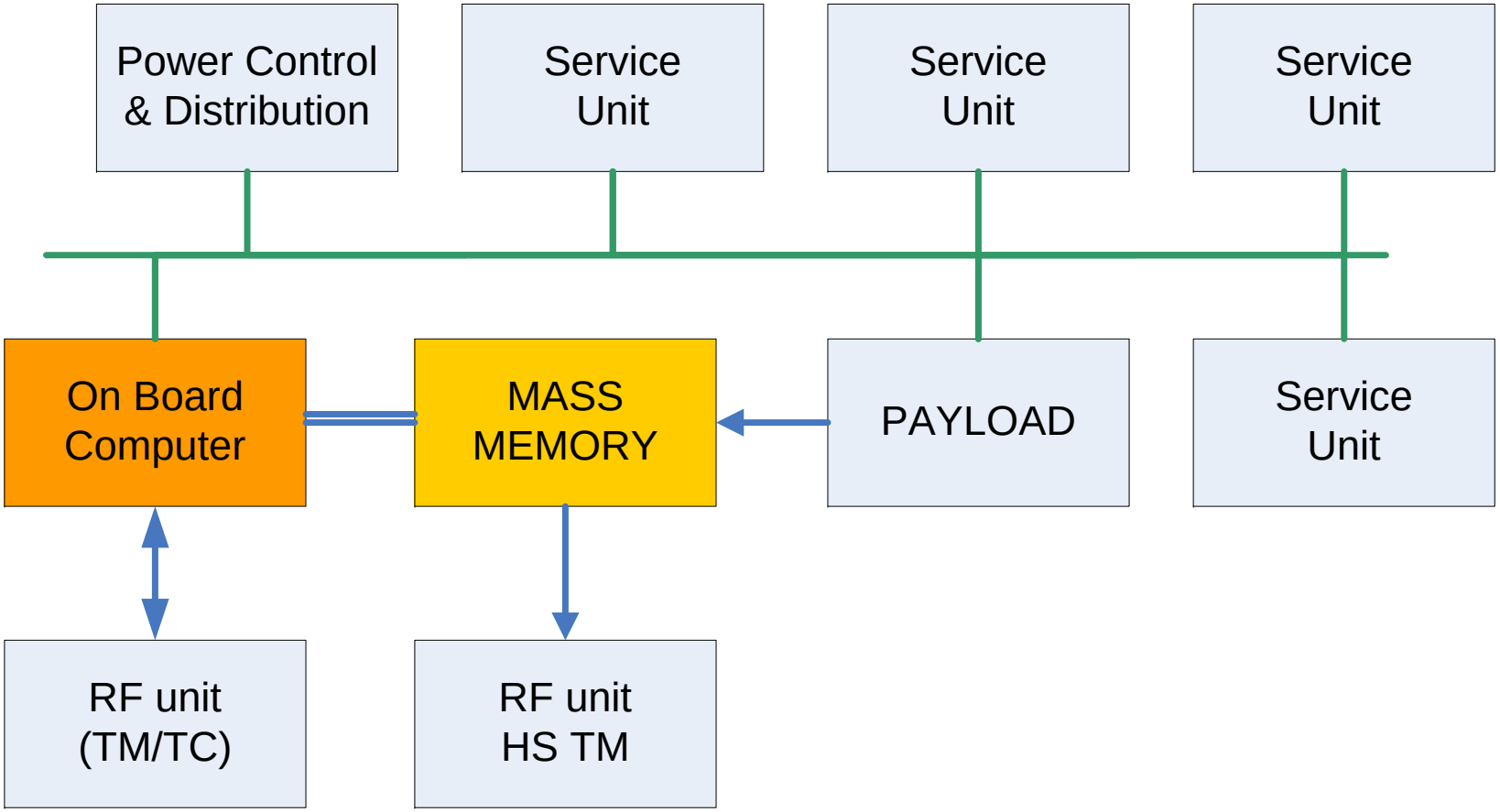
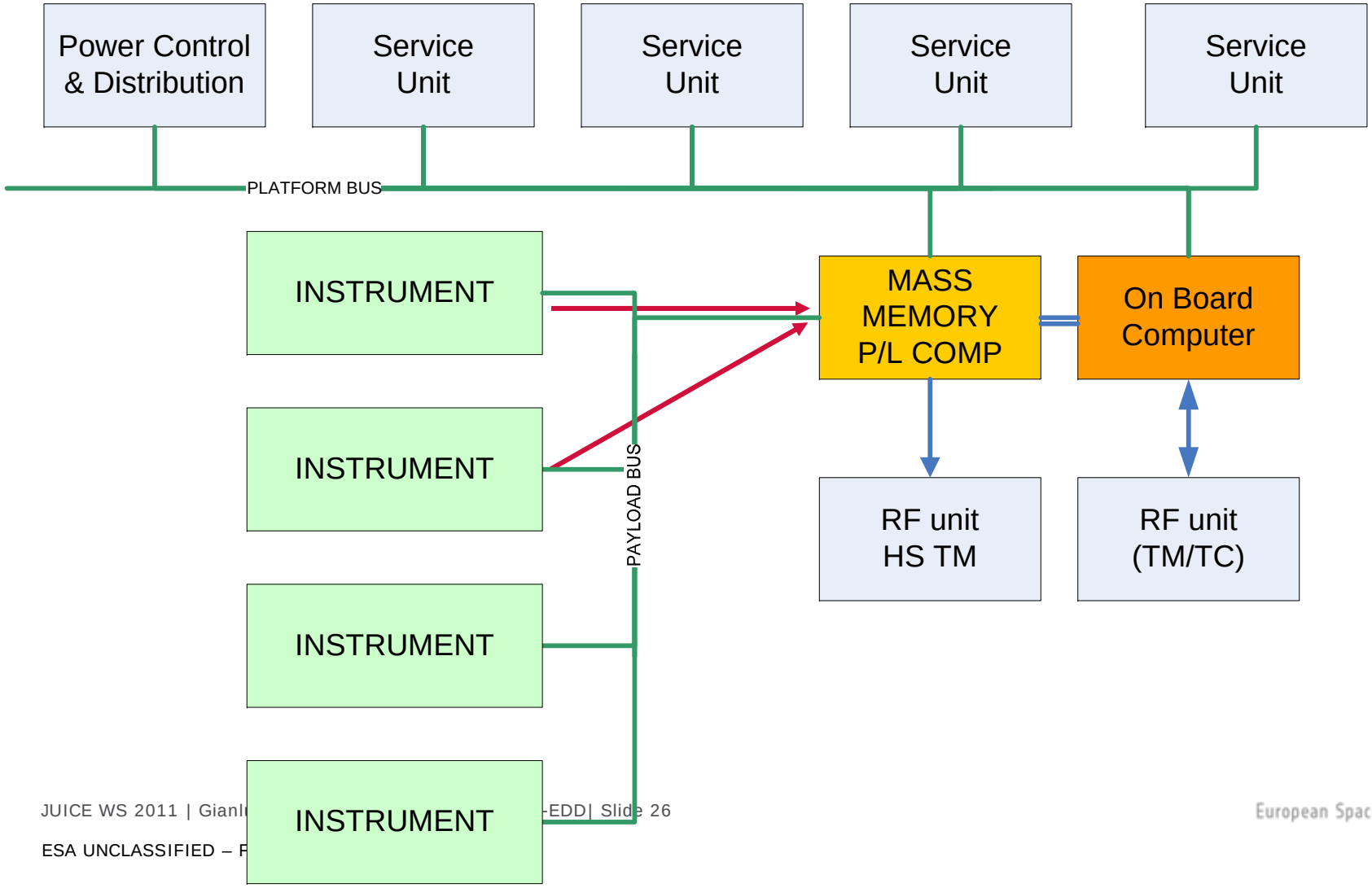
Payload view of S/C reference architecture (I)

1. ‘few instruments’ case

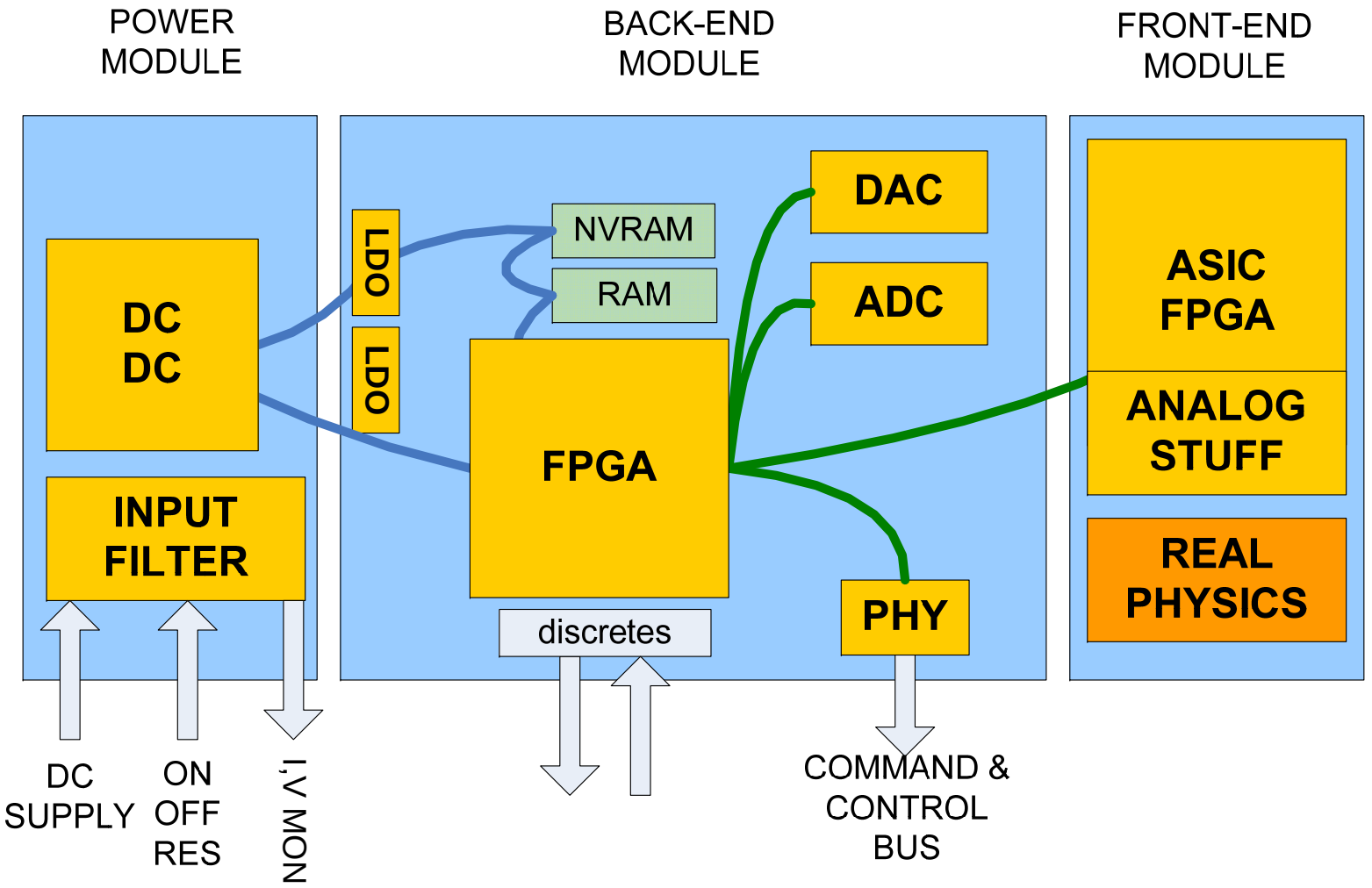


Payload view of S/C reference architecture (II)

1. Many instruments case

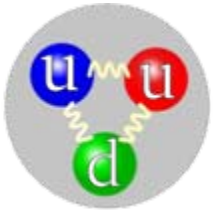


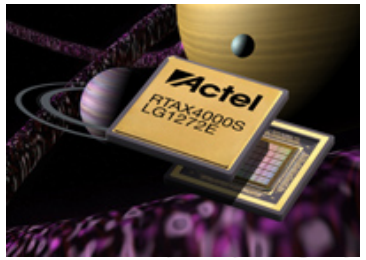
Designing an instrument, the starting point



Designing an instrument, reality check

- With a TID requirement of 100 Krad (equivalent to 15-year telecom) there's only one possible choice for FPGA: Microsemi (ACTEL) antifuse
- Antifuse FPGAs are live-at-power-on, they don't need additional NVRAM to store code ☺
- Antifuse FPGAs are one time programmable ☹
- Antifuse FPGAs are power hungry (and dual power…) ☹
- Antifuse FPGAs are ITAR 😐
- Latest generation antifuse FPGAs come in HUGE packages (TQFP 256/352 … unless you are able to mount CCGA624 ;-) ☹
- Latest generation Antifuse come with a relatively 'soft' embedded RAM. EDAC is mandatory. 😐



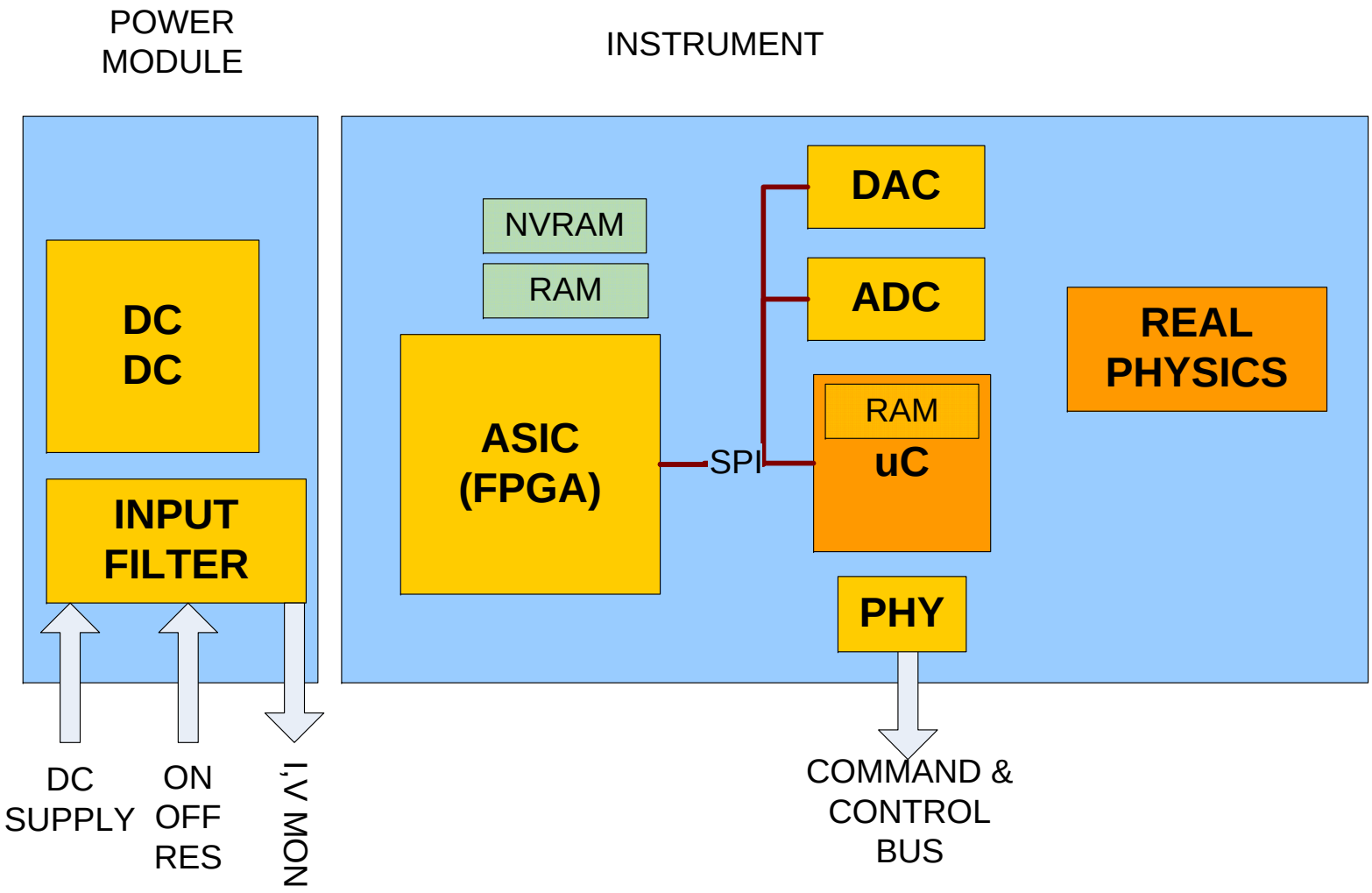


Why all this fuss about FPGAs ?

FPGAs should be forbidden in space applications until the designers learn how to design with them (Sandi Habinc, when still at ESA)

- Use of FPGA in a design always often leads to not optimized designs
- Complex SoC in FPGA (expecially in OTP FPGAs) are as difficult to test as in ASIC
- FPGA have high recurrent costs
- Again, little choice in the market, you make your design (and schedule) dependent from non engineers

The same design as before, just better



Why better ? (cont)

1. Use of standard busses

   AMBA (AHB/APB) for IP cores inside ASIC/FPGA

   SPI for module level interconnection

   CAN/Spacewire for the external world

   right-first-time development of this system should be easier,

   Makes system technology independent, to allow reuse of IP cores, peripherals and system macrocells across diverse IC processes, component manufacturers …

   encourages modular system design to improve testability and the development of reusable peripheral and system IP libraries

   minimizes overheads (pin count is more important than FPGA space) while supporting high performance and low power on-chip communication.

   allows safer use of COTS components

Why better ? (more …)

2. Focuses on what instrument developers know best: INSTRUMENT CORE

Instrument development can be easily made parallel

(you DON'T need the final ASIC to develop your detector EM)

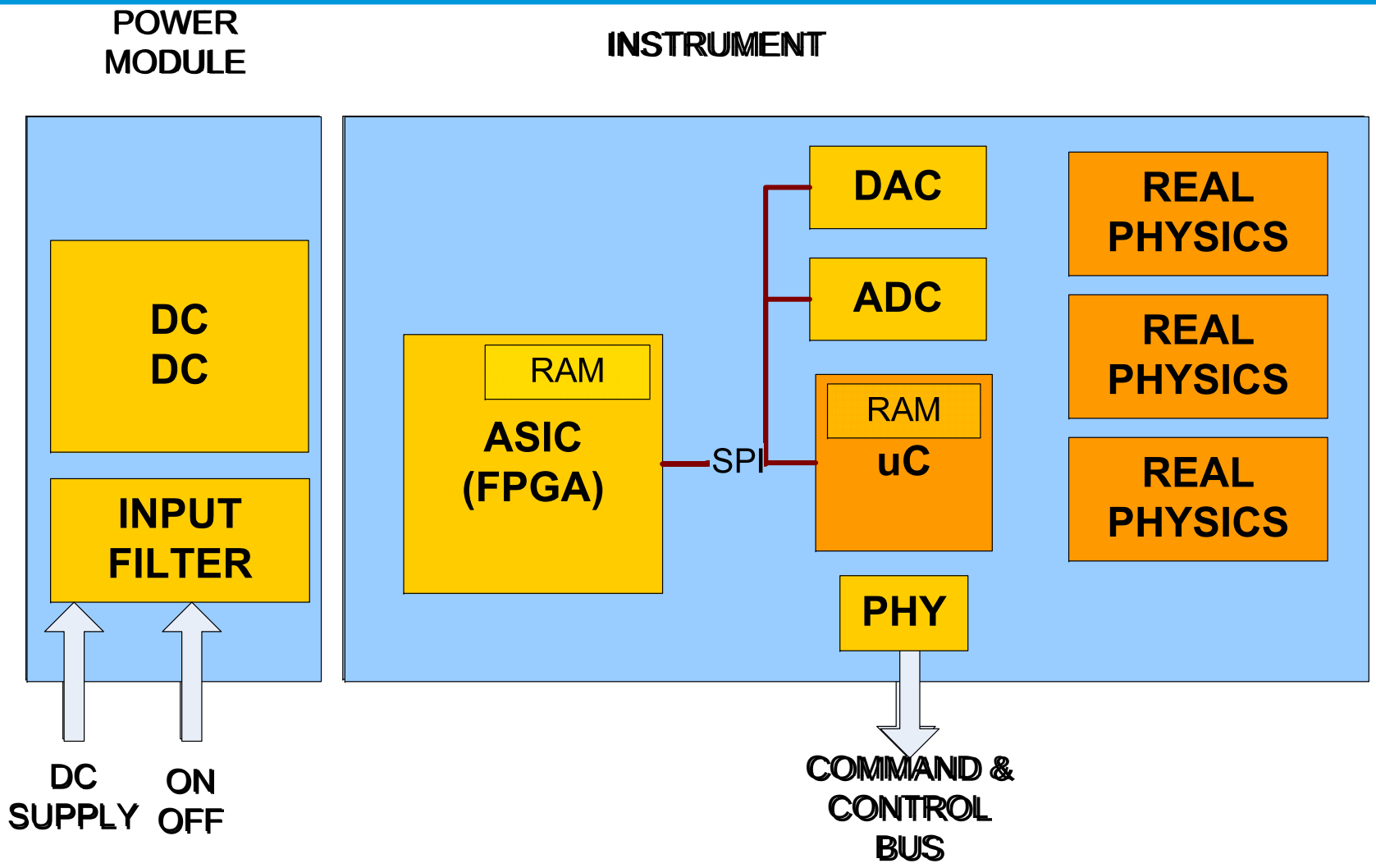
"standardized" designs are easier to integrate and assess/evaluate also from Prime/ESA side (and, in general, reduce risks)

It allows RESOURCE SHARING, with parallel developments

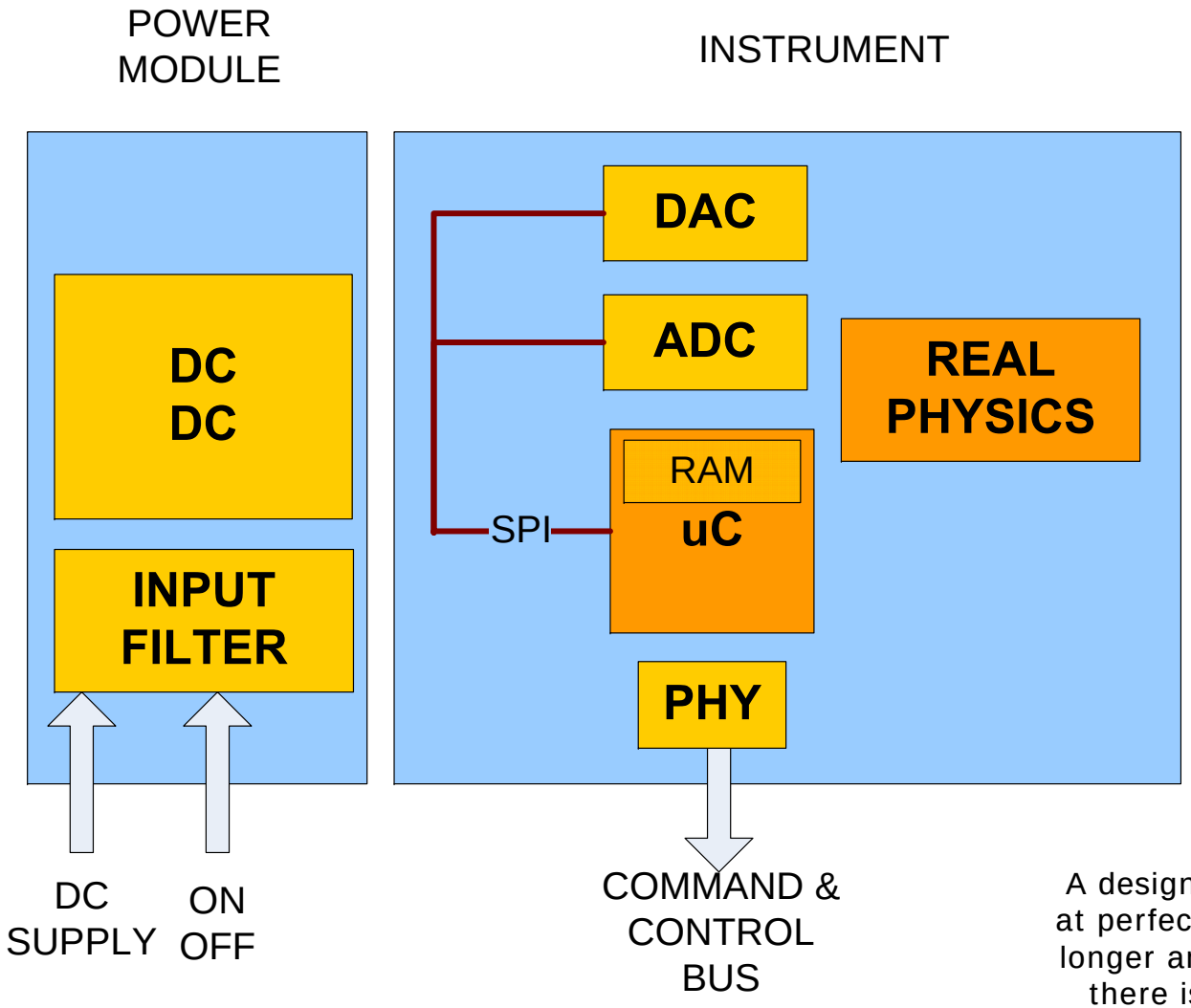
What is not there will not break

(S. Korolev)

Designs can be further optimized



Some instruments may have lesser needs…



A designer knows he has arrived at perfection not when there is no longer anything to add, but when there is no longer anything to take away.
(Antoine de Saint-Exupery)

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NVRAMs are a key design case

1. There's not such thing as a 'space grade' NVRAM
2. Commercial markets are dominated by NAND (and some NOR) FLASH
    a. Due to its relatively simple structure and high demand for higher capacity, NAND flash memory is the most aggressively scaled technology among electronic devices.
    b. The technology has reached 20 nm in production (SAMSUNG, INTEL, MICRON). While the expected shrink timeline is a factor of two every three years per original version of Moore's law, this has recently been accelerated in the case of NAND flash to a factor of two every two years.
    c. As the feature size of flash memory cells reach the minimum limit further flash density increases will be driven by greater levels of MLC, possibly 3-D stacking of transistors, and improvements to the manufacturing process.
    d. The decrease in endurance and increase in uncorrectable bit error rates that accompany feature size shrinking shall then be compensated by improved error correction mechanisms.

FLASH Memory standardization

A group called the **Open NAND Flash Interface Working Group** (**ONFI**) has developed a standardized low-level interface for NAND flash chips. This allows interoperability between conforming NAND devices from different vendors. The ONFI specification version 1.0 was released in 2007.

It specifies:

- a standard physical interface (pinout) for NAND flash in TSOP-48, WSOP-48, LGA-52, and BGA-63 packages
- a standard command set for reading, writing, and erasing NAND flash chips
- a mechanism for self-identification

The ONFI group is supported by major NAND flash manufacturers, including Hynix, Intel, Micron Technology, and Numonyx, as well as by major manufacturers of devices incorporating NAND flash chips

SAMSUNG is not ONFI, but almost…

FLASH – Radiation effects

On top of errors due to feature shrinking on (SLC NAND) FLASH devices we have to add errors induced by radiation exposure

Veronique will entertain you on the subject soon

In general:

- TID (and NIEL) related errors
- SEE errors

Latch-up and micro-latchup conditions have been observed by many experiments as a step increases in standby current indicate successive micro latchup conditions.

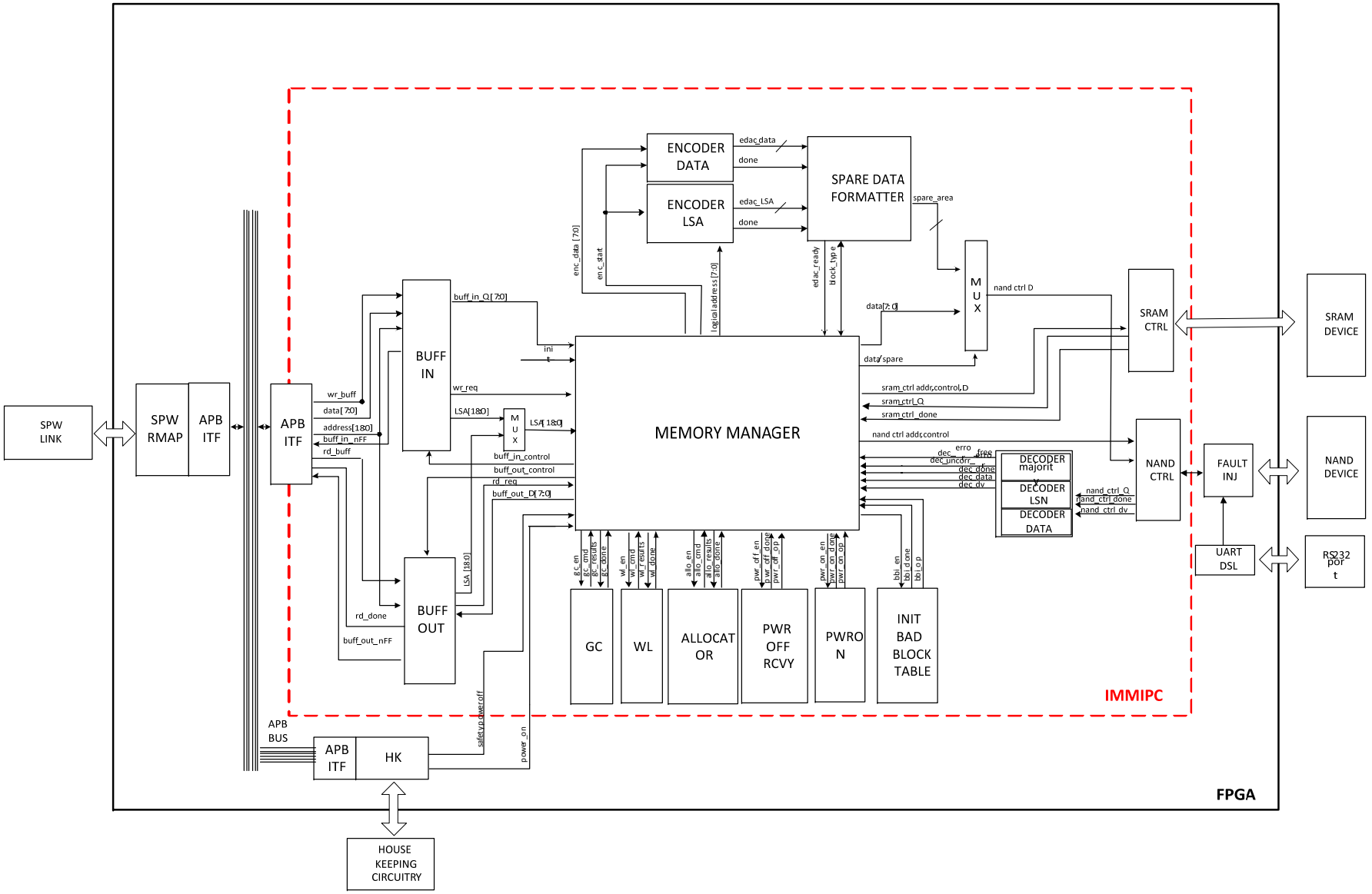
While single event upsets or multi-bit upsets performances are deteriorating at lower voltage supplies, SEL improves at lower voltage and latchup is eliminated below the latchup holding voltage.

On the opposite side, shrinking features play a 'helping' role for SEUs (actually reducing cross section) but increase importance of micro-latchup effects.

Flash Translation Layer

1. Bulding on device standardization (so we can be rather independent from future evolutions of FLASH technology) we can think about providing a standard FTL for all future flash memories.
2. This component (in form of an IP) will allow safe use of any (ONFI, for the moment) FLASH array boosting their overall (U)BER performance due to ageing and radiation.
3. The component takes care of all the FLASH management
    a. Wear leveling
    b. Buffering
    c. Paging
    d. Physical/Logical traslation
    e. Garbage collection
    f. Advanced transparent ECC (based on BCH codes)
    g. Block level peripheral access

Juice Flash controller IP – block scheme



FLASH FTL IP – Resources (preliminary)

12% SpWRMAP + AMBA

3% buffer in/out

>12% FTL (not yet complete)

15% ENCODER/DECODER

Of a ProAsic3 A3PE3000 (roughly equivalent to a RTAX2000).

So, this is not only for the central processor/memory but can be used for instrument buffers.

The Inconvenient Truths

NAND Flash Memories

1. are not NVRAM
2. ARE NOT NVRAM
3. ARE DEFINITELY NOT NVRAM
4. have different failure modes from RAM
5. needs digital latch-up and functional protection + redundancy
6. go fast! (i.e., scaling a factor 2 each 2 years)
7. have to provide compatibility with OSes and at device replacement level
8. have a design complexity strictly related to the usage scenario

So, don't carry your Ipod to Jupiter. Warranty won't cover it.

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ESA (Data Systems) developments of interest

1. IP Cores (and VHDL modeling guidelines…)
    a. Communication
    b. Processing
    c. Image compression
2. Microcontroller
3. Present processors
4. Future processors
5. Physical layer serial digital
    a. Specs
    b. Chips (CAN, 1553 …)
6. ‘Known good’ parts and design method
    a. POL
    b. FDIR
7. RASTA test and breadboarding system
    a. Software

What I expect

1. Many developments are ongoing, so there's still time to inject requirements
    a. A good example is the microcontroller

2. If any specific (e.g. communication) IP is needed this is the time to speak up

3. If there is any specific COTS component needed for any particular use, make it clear already at proposal time. As I underlined when talking about FLASH, using COTS around Jupiter requires DESIGN solutions that go beyond simple radiation tests (that are anyhow a fundamental prerequisite).

4. If an FPGA is deemed necessary for your instrument include in the proposal a trade off between FPGA and ASIC.

THANK YOU !