# DARE+

## Design Against Radiation Effects
## (Digital) Cell Libraries

## Jupiter Icy Moons Explorer (JUICE)
## Instruments Workshop
## 9 November 2011

# Objectives (1/2)

**Provide a suitable and mixed-signal capable microelectronic technology for platform and payload elements of S/C on Jovian missions.**

**Increase and demonstrate the maturity of the existing DARE 180 nm library for applications in very harsh radiation environments up to 1 Mrad TID (Si).**

# Objectives (2/2)

- Create currently missing library elements.
- Fix known issues.
- Create standard packaging solutions.
- Design, manufacture and evaluate a test vehicle.
- Design, manufacture and evaluate a representative ASIC.

# DARE

## Design Against Radiation Effects
## (Digital) Cell Libraries

# Space ASICs in Europe: **Old & Recent challenges**

**LOW VOLUMES:** no big profits with space ASICs

**EXPENSIVE SPACE QUAL CONTROL** (rad effects, reliability make more design and tests necessary; Agencies periodic audits)

**PACKAGING:** still to be qualified for space: flip-chip and column/short pin packages for high pin counts. Also PCB mounting. Space ASICs tend to be large…

**Big Uncertainties on EU ASIC Fabs future:**

- **ATMEL(F)** is selling its last plant in Europe (Rousset), after selling plants in France (MHS), UK and Germany. The whole ASIC Business Unit might be sold as well. Sales declines forced to temporary foundry shuts.
- **E2V(F)** is restructuring internally due to revenue decline. Temporary shuts.
- **XFAB** fab in UK closing
- **LFOUNDRY (D)** fab in Landshut is closed. Future of Rousset plant (see above) is uncertain.

# Why DARE was created

- **late 90's** ASIC Foundries used for space components were scarce, expensive and were discontinuing rad hard processes (ABB-HAFO & SOS). The dependence on commercial, high volume ASIC processes was evident.

- **1999:** First Technology Research Programme (TRP) funds were dedicated to Harden-by-Design ASIC libraries based on a commercial technology: UMC 180nm available on Europractice MPW.

- **2000/2001**After 1st proof of concept, new contracts launched to improve and add library elements, and develop a 1st customer design (DROM).

- **2006/07** new contracts launched to do a second customer design (LEON3), including ESCC evaluation and a maintenance contract, to start porting DARE to 90nm.

:

**Closed**:

| | | |
|---|---|---|
| • 14177/99/NL/FM | GSTP-2 | Proof of concept |
| • 14932/00/NL/DS | NSGU | Main Library Development |
| • 15852/01/NL/FM | TRP | Radiation Hardening by Design (RHBD) 3 |

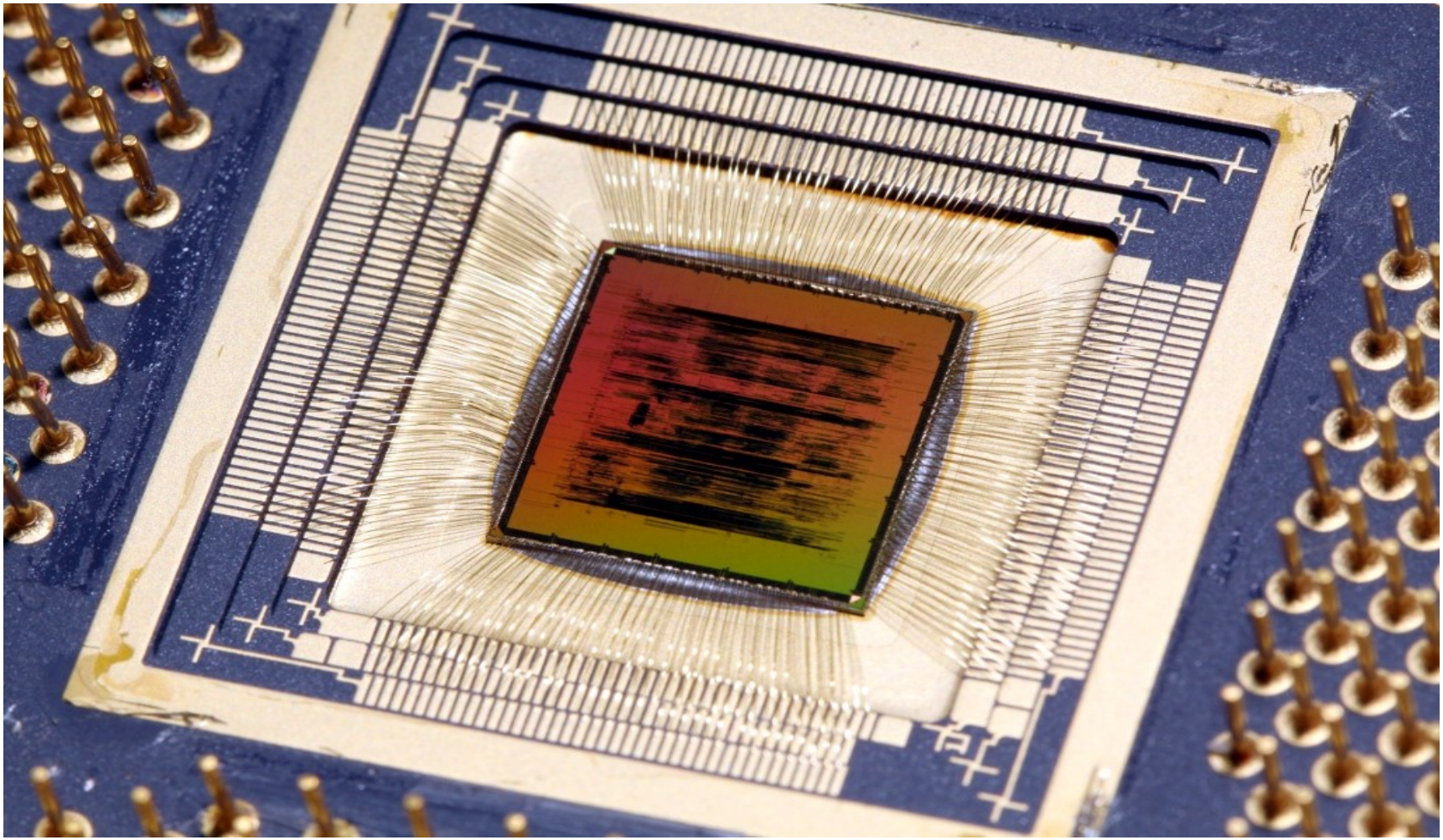
**On-going:**

| | | |
|---|---|---|
| • 19916/06/NL/JD | GSTP | ASICs for Space Fabricated with RHBD Library |
| • 20896/07/NL/JD | TRP | DARE Maintenance and Porting |
| • 4000Xxxxxx | TRP | DARE+ |

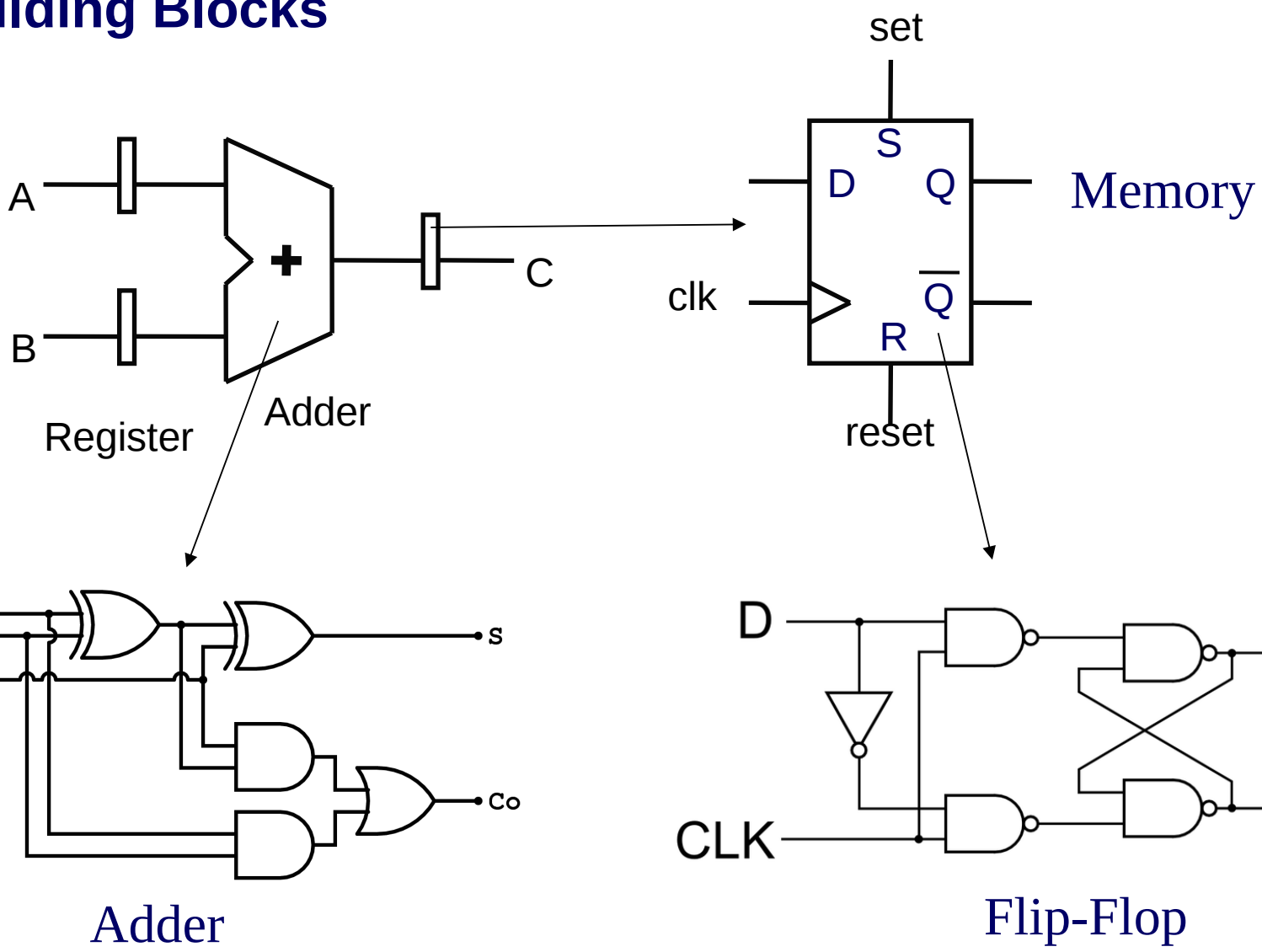
**Related:**

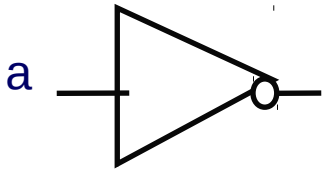
| | | |
|---|---|---|
| • 21855/09/NL/JK | TRP | Radiation Effects on Deep Sub Micron CMOS Technologies |

# Integrated Circuits

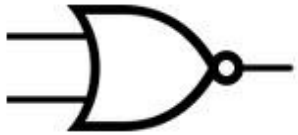


# Building Blocks

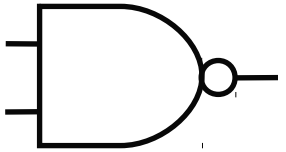




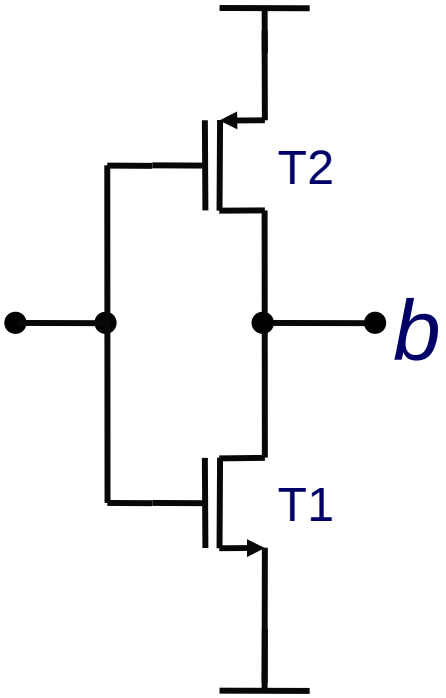

Inverter

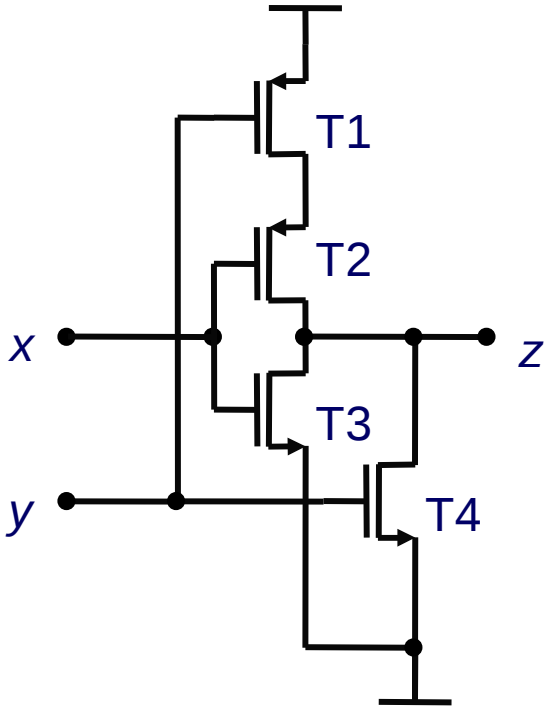


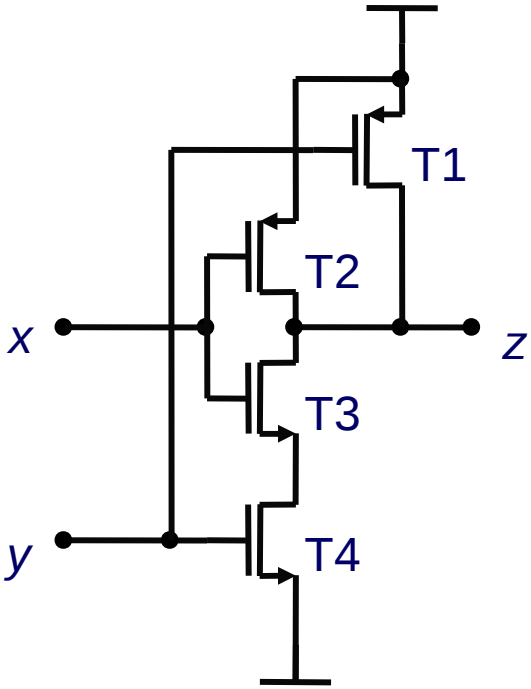
NOR



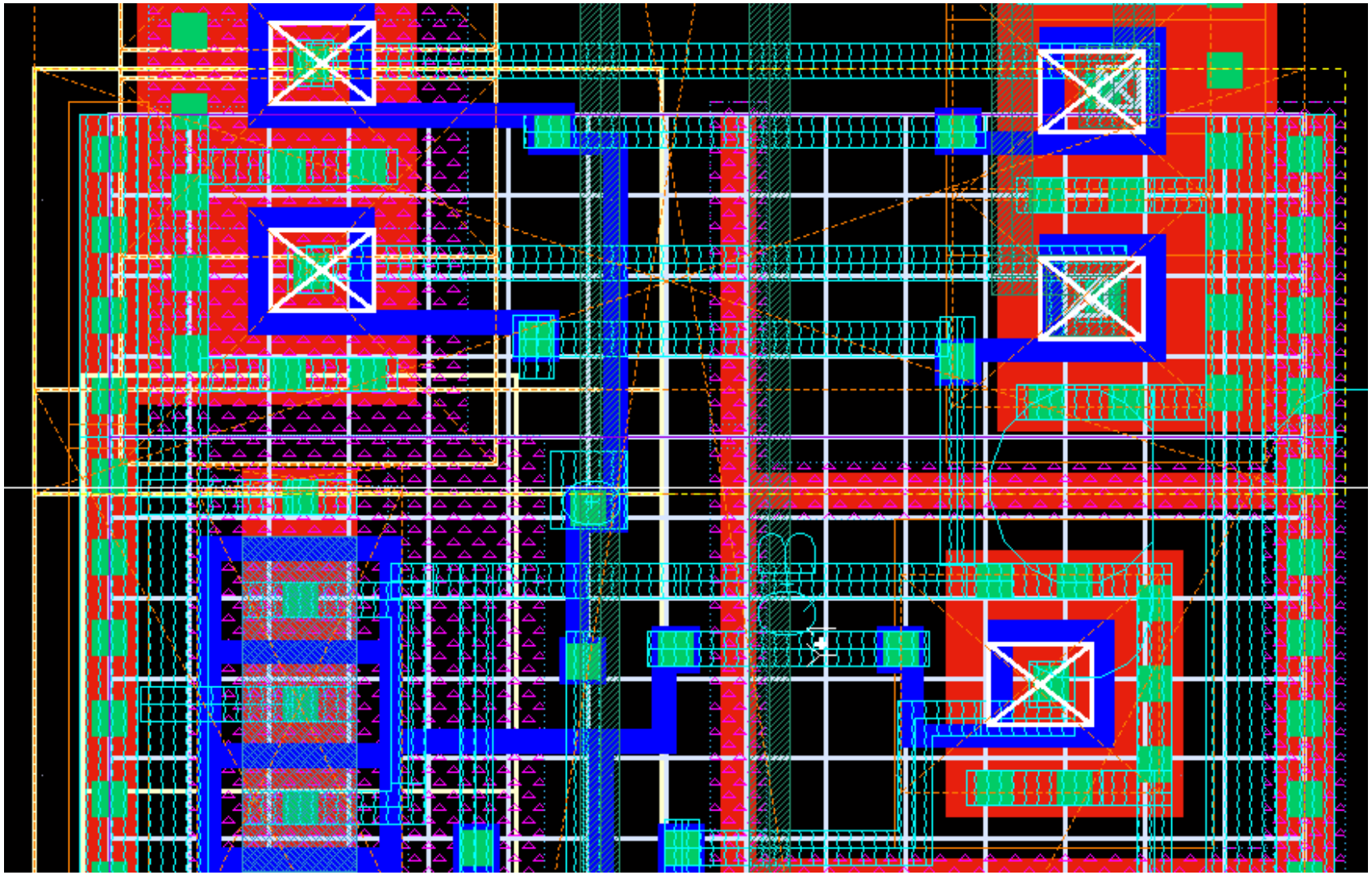
NAND



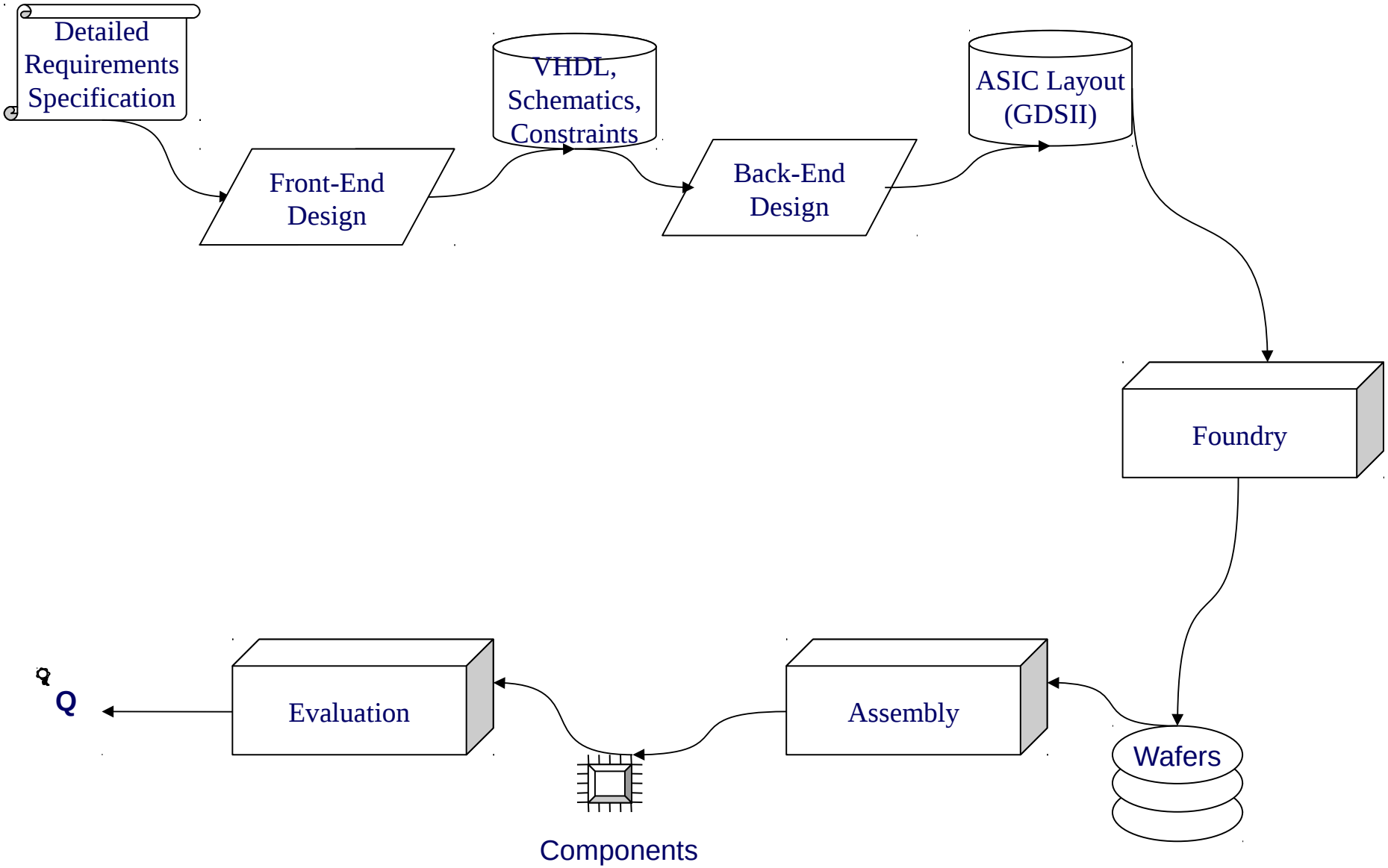



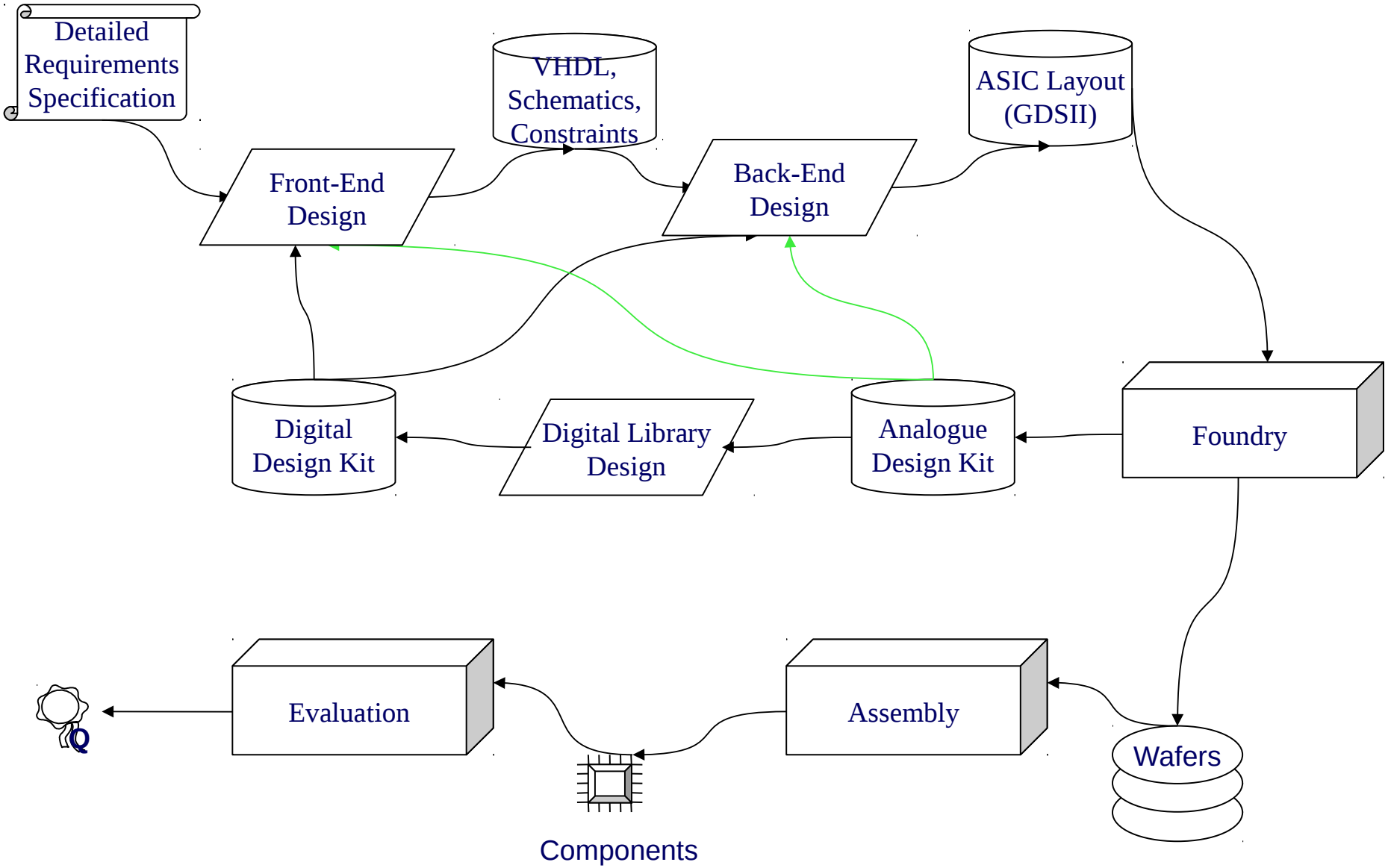
# Layout (part of XDFF)



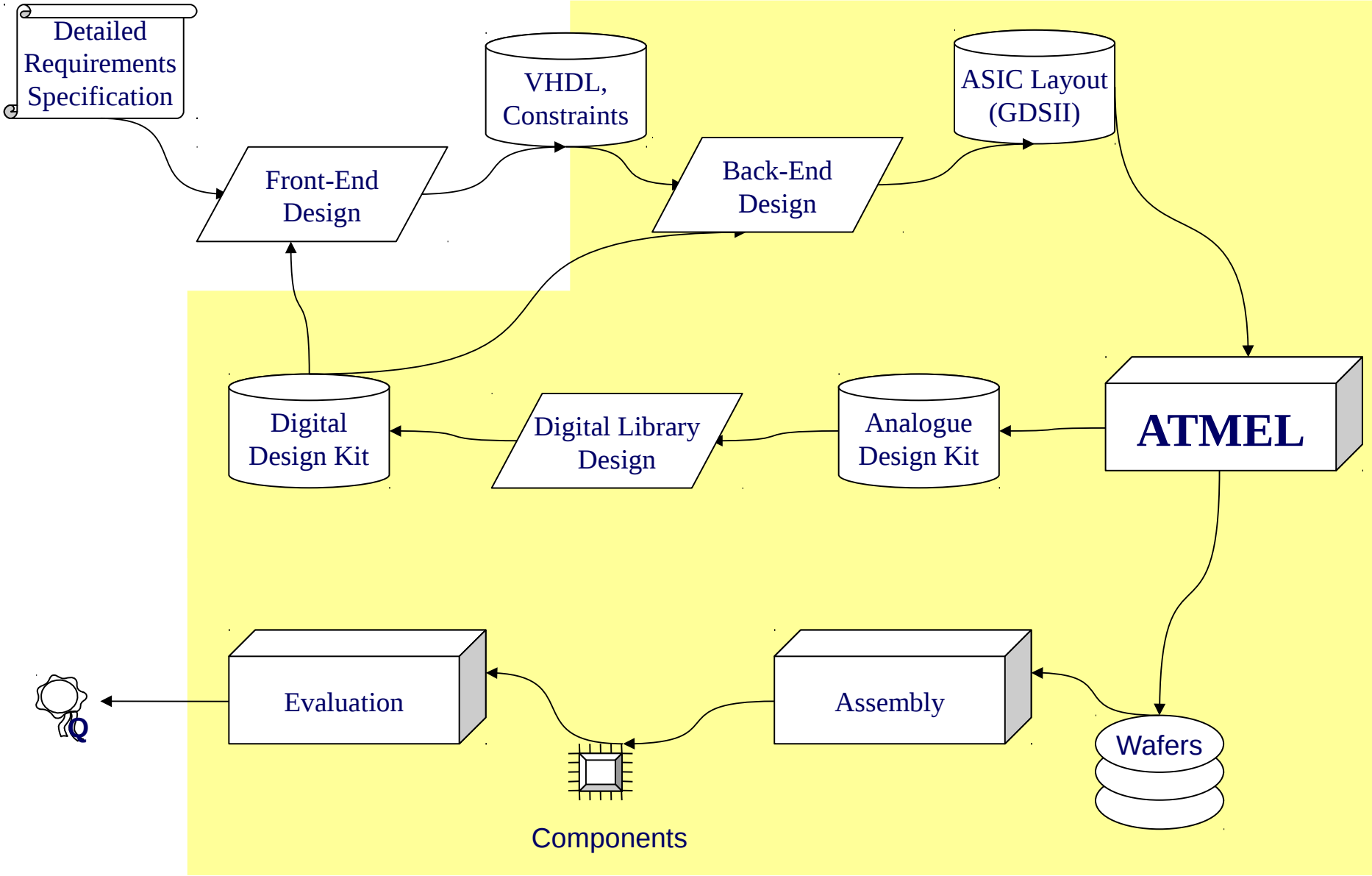
# ASIC Flow: Design, Manufacture and Test



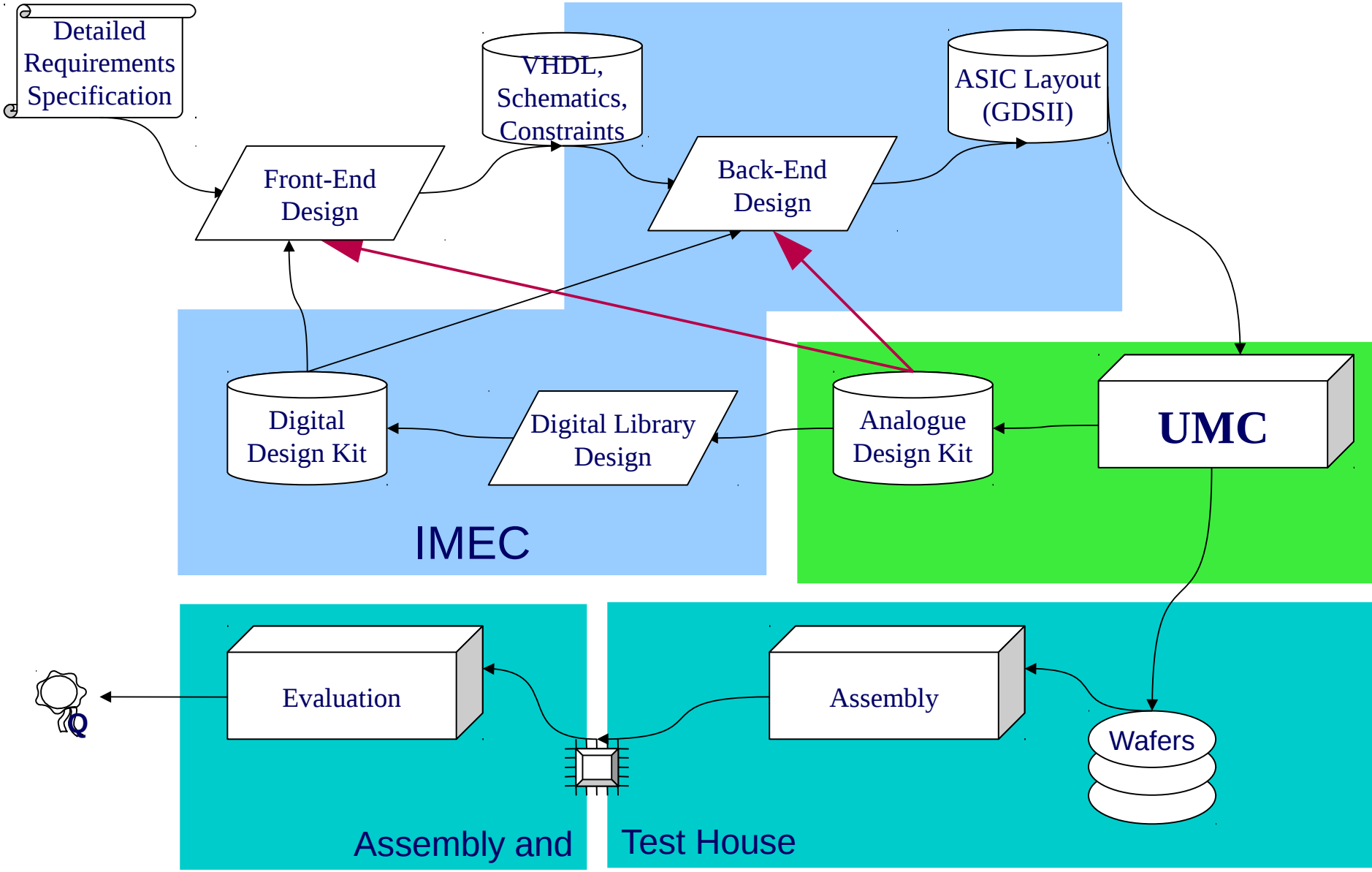
# ASIC Flow: Design Kits



# ASIC Flow: ATMEL



# ASIC Flow: DARE 180 nm / 90 nm



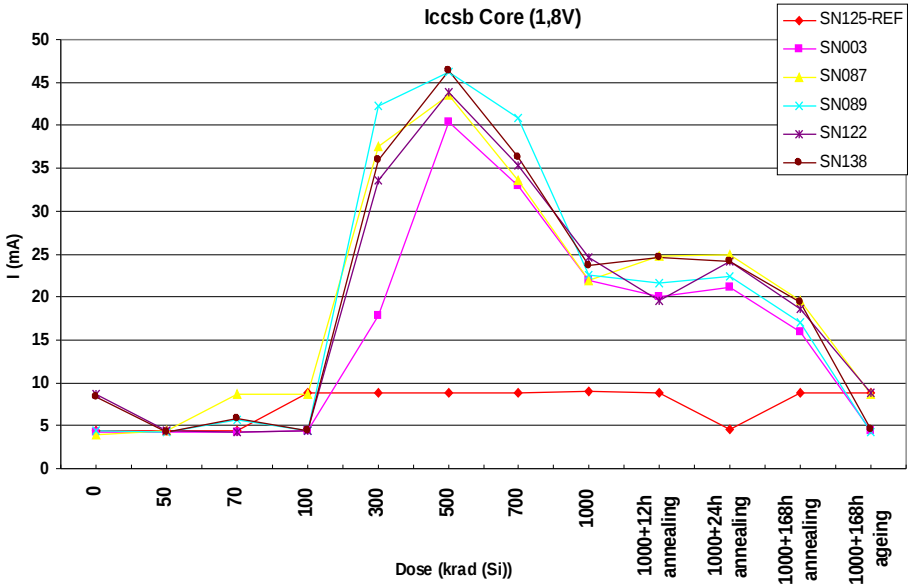
# TID test (1/2)

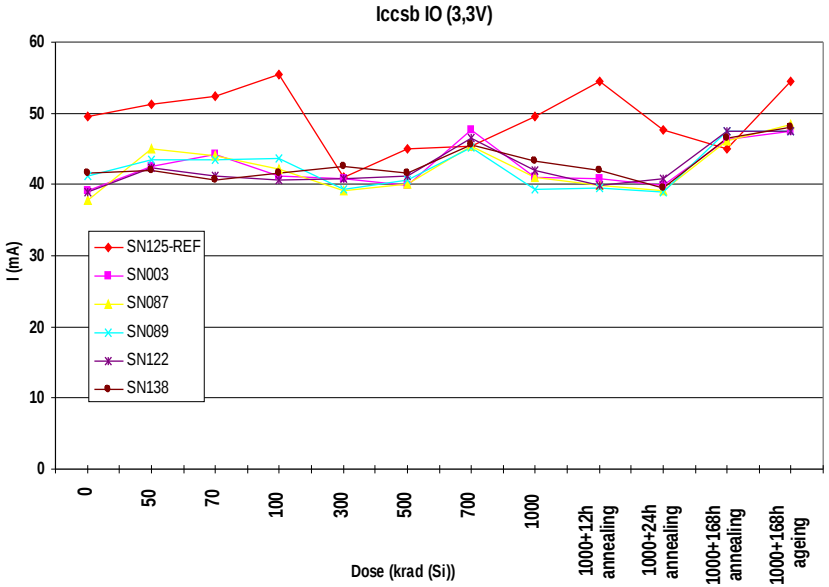
- Following ESCC22900
- Icc stand-by of the core :
  Stable until 100 krad(Si)

  Increase until 500 krad (Si)

  To decrease until 1 Mrad (Si)

  Fully recovery & functional after accelerated ageing at 100 °C



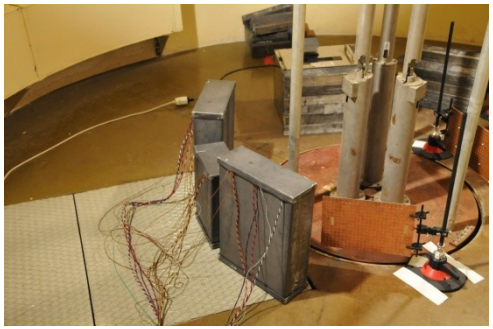



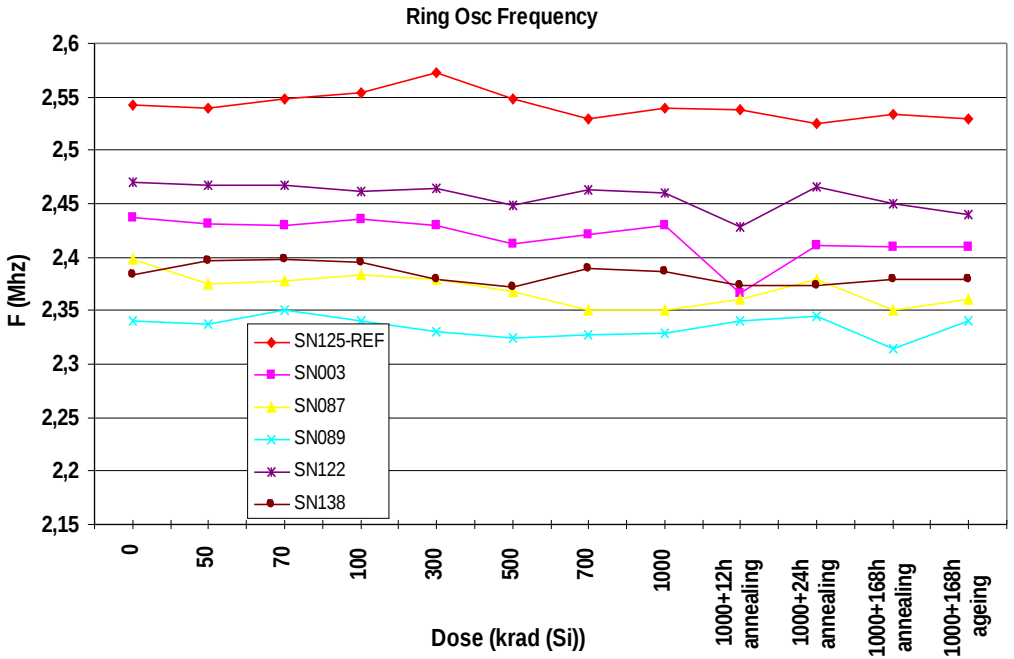

- **Icc stand-by of the IO :**
  - Dominated by the LVDS buffers consumptions
  - No significant evolution during the irradiation

# TID test (2/2)

- Timing drift :
  Measure of an embedded ring oscillator

  No significant variations during and after irradiation





# DARE +

## Design Against Radiation Effects
## (Digital) Cell Libraries
## for Harsh Space Environments

# DARE+

- Core Library
  - Clock gating
  - 3.3 V flavor
- RAM compiler
  - Problem fix
  - Dual port
- PLL
  - Full characterization
- Re-characterization for mixed-mode technology flavor

- I/O Library
  - 5V tolerant
  - Pull-up / pull-down
  - Improved LVDS
  - Improved ESD protection
  - Multi fan-out
  - IBIS Models
- **3.3 V -> 1.8 V voltage regulator**
- **Demonstration ASIC (DSP)**

# PLL

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Junction Temperature | | -55 | - | 145 | °C |
| Supply Voltage | | 1.62 | 1.8 | 1.98 | V |
| Power, Analog Supply | | - | - | 1 | mA |
| Power, Digital Supply | | - | - | 0.5 | mA |
| Input Frequency (1) | | - | 50 | - | MHz |
| Output Frequencies (1) | FX4<br>FX2<br>FX1 | - | 200<br>100<br>50 | - | MHz |
| Duty Cycle; for all three outputs FX4, FX2, FX1 | | 49 | - | 51 | % |
| Phase Error | | -100 | - | 100 | pS |
| Cycle to Cycle Jitter | | -100 | - | 100 | pS |
| Long Term Jitter | | -200 | - | 200 | pS |
| Lock Time | | - | 25 | 100 | µS |
| Output Load | | - | - | 0.8 | pF |

# SRAM (Compiler)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Junction Temperature | -55 | - | 145 | °C |
| Supply Voltage | 1.62 | 1.8 | 1.98 | V |
| SRAM Size | 256 | - | 262144 | bit |
| Operating Frequency | - | - | 200 | MHz |

# 5V Tolerant I/O

| Cell Name | Description | Pins | | | |
|---|---|---|---|---|---|
| | | Input | Enable | Output | PAD |
| **5V tolerant, 3.3V I/O** | | | | | |
| BICM3V5VT4 | 5V tolerant, 3.3V CMOS/LVTTL Bi-directional pad, drive = 4 mA | A | EN | Z | IO |
| BICM3V5VT8 | 5V tolerant, 3.3V CMOS/LVTTL Bi-directional pad, drive = 8 mA | A | EN | Z | IO |
| BICM3V5VT12 | 5V tolerant, 3.3V CMOS/LVTTL Bi-directional pad, drive = 12 mA | A | EN | Z | IO |
| BICM3V5VT16 | 5V tolerant, 3.3V CMOS/LVTTL Bi-directional pad, drive = 16 mA | A | EN | Z | IO |
| BICM3V5VT24 | 5V tolerant, 3.3V CMOS/LVTTL Bi-directional pad, drive = 24 mA | A | EN | Z | IO |
| | | | | | |
| ITTL3V5VT | 5V tolerant, 3.3V CMOS/LVTTL input pad | A | EN | Z | IO |

| Parameter | Description | CMOS | | LVTTL | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| $V_{IL}$ | Low-level input voltage | | 0.3*v33io | | 0.8 V |
| $V_{IH}$ | High-level input voltage | 0.7*v33io | | 2 V | |

# Output Pads w/ Slew Control

| Cell Name | Description | Pins | | | |
|---|---|---|---|---|---|
| | | Input | Enable | Output | PAD |
| **3.3V I/O** | | | | | |
| OCMTR4 | 3.3V Tri-state CMOS/LVTTL output pad, drive = 4 mA | A | EN | | Z |
| OCMTR12 | 3.3V Tri-state CMOS/LVTTL output pad, drive = 12 mA | A | EN | | Z |
| OCMTR24 | 3.3V Tri-state CMOS/LVTTL output pad, drive = 24 mA | A | EN | | Z |
| | | | | | |
| OCM3V4 | 3.3V CMOS/LVTTL output pad, drive = 4 mA | A | | | Z |
| OCM3V12 | 3.3V CMOS/LVTTL output pad, drive = 12 mA | A | | | Z |
| OCM3V24 | 3.3V CMOS/LVTTL output pad, drive = 24 mA | A | | | Z |
| | | | | | |
| BICM3V4 | 3.3V CMOS/LVTTL Bi-directional pad, drive = 4 mA | A | EN | Z | IO |
| BICM3V12 | 3.3V CMOS/LVTTL Bi-directional pad, drive = 12 mA | A | EN | Z | IO |
| BICM3V24 | 3.3V CMOS/LVTTL Bi-directional pad, drive = 24 mA | A | EN | Z | IO |
| **2.5V I/O** | | | | | |
| OCM25VS | 2.5 V CMOS output pad, Small drive | A | | | Z |
| OCM25VM | 2.5 V CMOS output pad, Medium drive | A | | | Z |
| OCM25VL | 2.5 V CMOS output pad, Large drive | A | | | Z |

# Output Pads w/ New Drive Strengths

| Cell Name | Description | Pins | | | |
|---|---|---|---|---|---|
| | | Input | Enable | Output | PAD |
| **3.3V I/O** | | | | | |
| OCMTR8 | 3.3V Tri-state CMOS/LVTTL output pad, drive = 8 mA | A | EN | | Z |
| OCMTR16 | 3.3V Tri-state CMOS/LVTTL output pad, drive = 16 mA | A | EN | | Z |
| | | | | | |
| OCM3V8 | 3.3V CMOS/LVTTL output pad, drive = 8 mA | A | | | Z |
| OCM3V16 | 3.3V CMOS/LVTTL output pad, drive = 16 mA | A | | | Z |
| | | | | | |
| BICM3V8 | 3.3V CMOS/LVTTL Bi-directional pad, drive = 8 mA | A | EN | Z | IO |
| BICM3V16 | 3.3V CMOS/LVTTL Bi-directional pad, drive = 16 mA | A | EN | Z | IO |

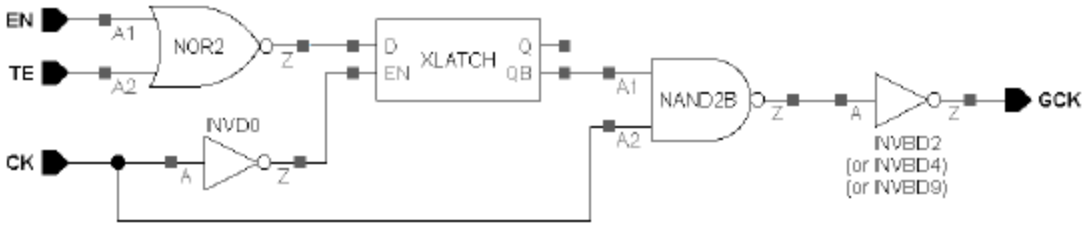
# Schmitt Trigger (2.5 / 3.3 V)

| Symbol | Parameter | Condition | Minimum | Maximum |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | – | 2.3V | 2.7V |
| Vt+ | Positive Going Threshold Voltage | $V_{OUT} \geq V_{OH(min)}$ | 0.9V | 1.7V |
| Vt- | Negative Going Threshold Voltage | $V_{OUT} \leq V_{OL(max)}$ | 0.7V | 1.5V |
| $V_{hyst}$ ($\Delta$Vt) | Hysteresis Voltage | Vt+ - Vt- | 0.2V | 1.0V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -2 mA | $V_{DD}$-0.45V | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2 mA | | 0.45V |

| Symbol | Parameter | Condition | Minimum | Maximum |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | – | 3.0V | 3.6V |
| Vt+ | Positive Going Threshold Voltage | $V_{OUT} \geq V_{OH(min)}$ | 0.9V | 2.1V |
| Vt- | Negative Going Threshold Voltage | $V_{OUT} \leq V_{OL(max)}$ | 0.7V | 1.9V |
| $V_{hyst}$ ($\Delta$Vt) | Hysteresis Voltage | Vt+ - Vt- | 0.2V | 1.4V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100 µA<br>$I_{OH}$ = -2 mA | $V_{DD}$-0.2V<br>2.4V | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100 µA<br>$I_{OL}$ = 2 mA | | 0.2V<br>0.4V |

# Integrated Clock Gating

| Cell Name | Drive Strength |
|---|---|
| XICG**D2** | 2x standard drive |
| XICG**D4** | 4x standard drive |
| XICG**D9** | 9x standard drive |



# Voltage Regulator

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Junction Temperature | -55 | - | 145 | °C |
| Input Voltage Range | 3.0 | 3.3 | 3.63 | V |
| Output Voltage Range | 1.62 | 1.8 | 1.98 | V |
| Output Voltage Accuracy | -2 | | 2 | % |
| Output Current | - | - | 50 | mA |
| Virtually Zero $I_Q$ (Disabled) | - | - | 50 | nA |
| Very Low $I_Q$ (Enabled) | - | 50 | - | µA |
| PSRR @ 1KHz | - | 50 | - | dB |
| Start Up Time | | | 100 | µs |

LVDS Receiver

ESD Update

IBIS Models

Dual Port SRAM Compiler

8ch Analogue Multiplexer

# Analogue Design Kit

- Layout PCell for ELT transistors
- LVS deck that recognizes ELT transistors and computes proper L and W
- An excel sheet to compute W/L given ELT layout dimensions

Further development will target:
- Cleaned-up the SKILL code (sklint)
- Support for custom symbol (CDF) with TID parameter for simulation
- Support for LVT transistors

# Test Vehicles (1/2)

## (1) Analogue Characterization

Contains active and passive devices for characterization, including radiation tolerance

## (2) Digital Characterization

Contains all new or modified digital cell elements for (re-) characterization, including radiation tolerance

# Devices Test Vehicle

| | |
|---|---|
| 1.8V nmos | N_18_MM, N_LV_18_MM, N_BPW_18_MM |
| 1.8V pmos | P_18_MM, P_18_LV_MM |
| 3.3V nmos | N_33_MM, N_BPW_33_MM |
| 3.3V pmos | P_33_MM |
| Bipolar | PNP_V50X50_MM, PNP_V100X100_MM |
| Diodes | DION_MM, DIOP_MM, DIONW_MM |

MOS transistor parameters:

- Threshold voltage shift
- Mismatch/offset voltage
- Leakage current
- Noise
- Mobility (max frequency)
- Breakdown voltage

Bipolar transistor parameters:

- Beta
- Noise
- Collector-Base leakage current
- Mismatch/offset voltage
- Transit time (max frequency)

Diode parameters:

- Reverse current
- Ideality factor
- Barrier potential

# Library Test Vehicle

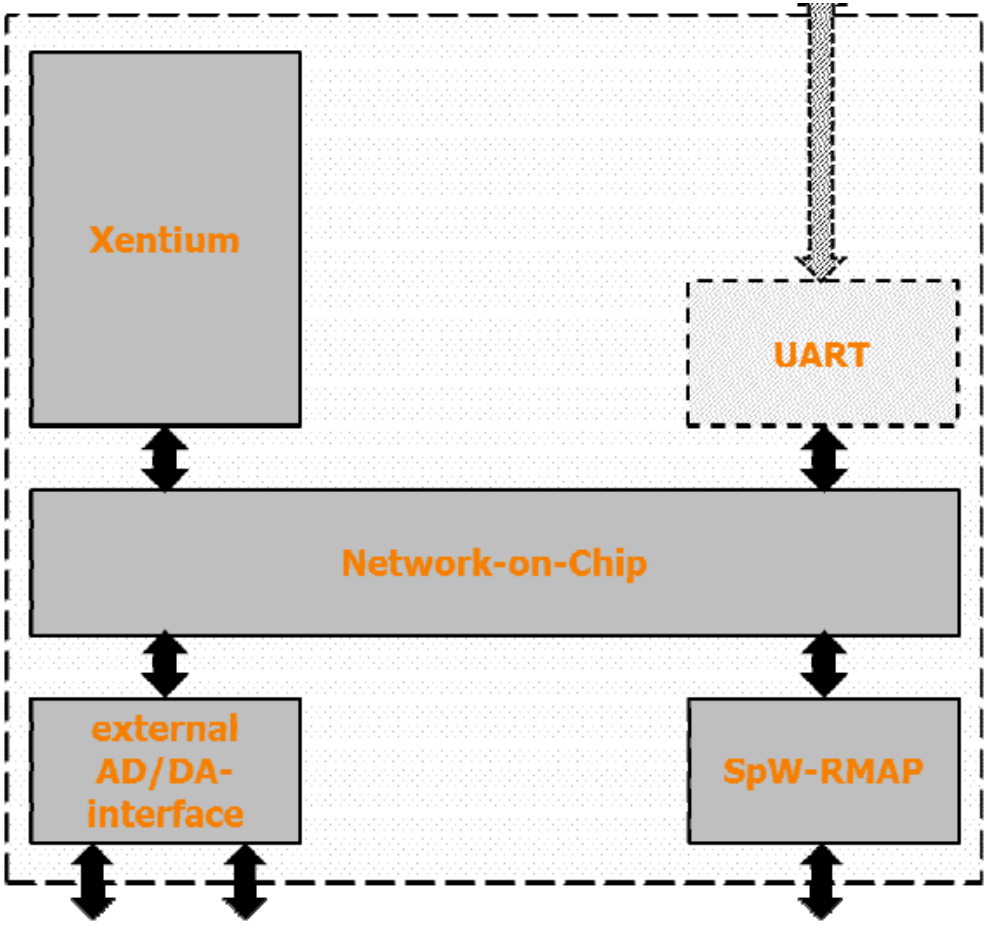
| Library element | Core area ($\mu m^2$) | I/O pins |
|---|---|---|
| CORE (ICG, SETfilter, ..) | 500000 | 20 |
| LVDS | 0 | 22 |
| I/O (functional/drive strength/IBIS) | 0 | 50 |
| I/O ESD (old + new) | 0 | 20 |
| Single Port sram128wx128b | 702432 | 12 |
| Single Port sram512wx64b | 1209369 | 12 |
| Single Port sram1024wx40b | 1491200 | 12 |
| Single Port sram1024wx16b | 667440 | 12 |
| Dual Port sram64wx16b | 167384 | 12 |
| PLL | 0 | 23 |
| Linear Voltage Regulator (3.3V → 1.8V) | 2000000 | 10 |
| Switched Voltage Regulator (3.3V → 1.8V) | 5000000 | 10 |
| reference circuits (UMC RO, single transistors, ELT/non-ELT) | 100000 | 20 |
| TID structures (ELT/GB variants, 128bit registers) | 200000 | 20 |
| SEE structures (SET filters, ROs, pulse propagation) | 200000 | 20 |
| SRAM subcells (MEM cells, timing measurement, small matrices with direct write/read access) | 1000000 | 20 |
| PLL subcells (VCO, divider, PFD) | 100000 | 10 |
| Voltage Regulator subcells (bandgap, comparator, switch, thermal diode) | 2000000 | 20 |

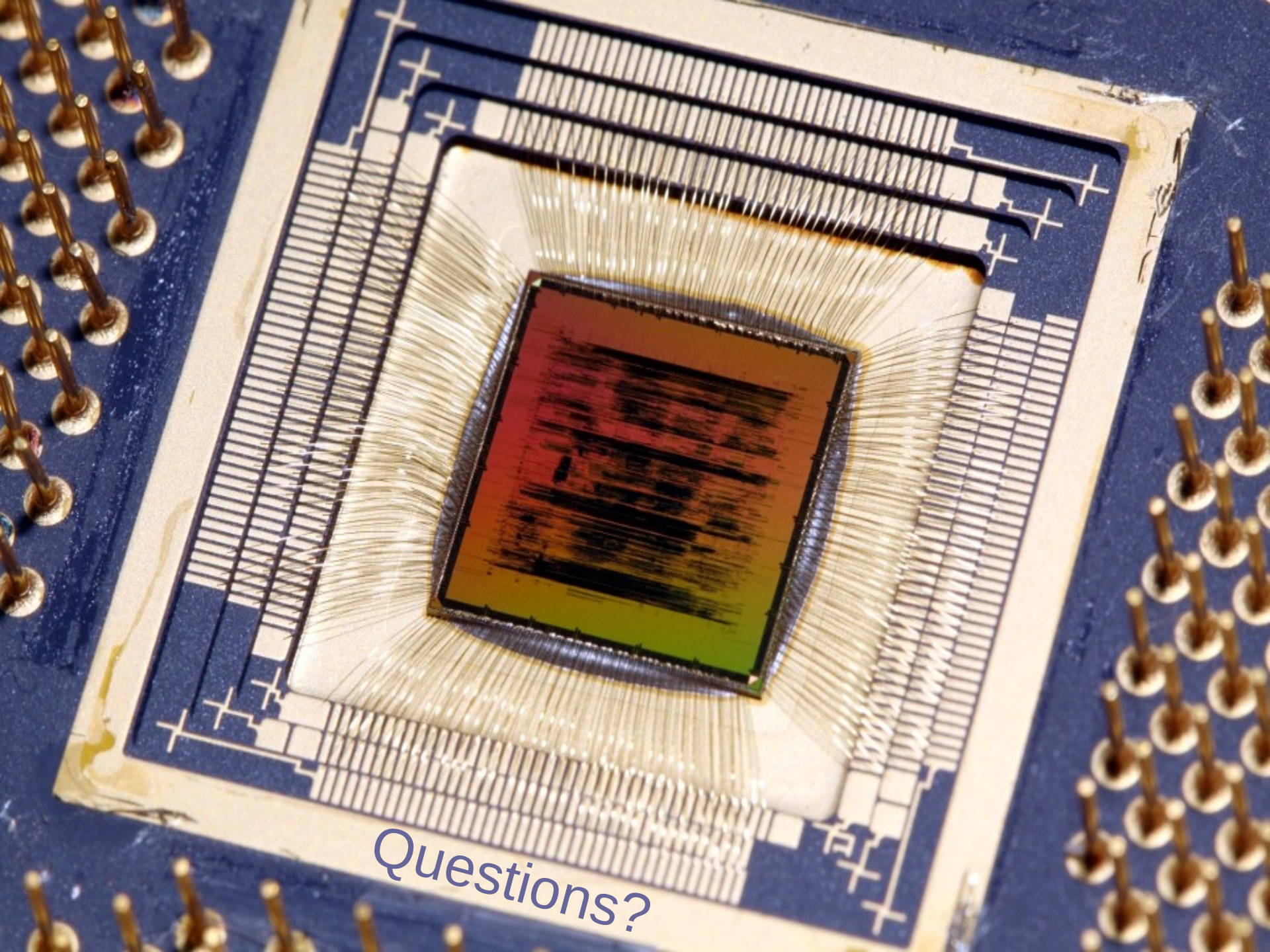
# Test Vehicles (2/2)

## (3) DSP

- Xentium VLIW DSP Core
- Network on chip
- SpaceWire I/F w/ RMAP
- Bridges for external ADC/DAC

Demonstration of Development Flow and tool compatibility




Questions?

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