# JUICE Instrument Workshop

Radiation Tolerant analogue / mixed signal technology survey and test vehicle design

Front-end readout ASIC technology study and development test vehicles for front-end readout ASICS

Richard Jansen

Estec

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# History

## Proposed activities

Radiation Tolerant analogue / mixed signal technology survey and test vehicle design

Front-end readout ASIC technology study and development test vehicles for front-end readout ASICS

## Motivation

Investigation of the ASIC process technology to meet radiation requirement for front-end readout circuits and mixed signal application

## Mission/Activity adjustment

Lowered the radiation requirement

Existing technology can meet the radiation requirement

Activity has been redefined to increase the output T.R.L.

## Development of MF and HF Configurable Instrumentation ASIC

Radiation tolerance 300krad – Applications: 100kHz - 100MHz
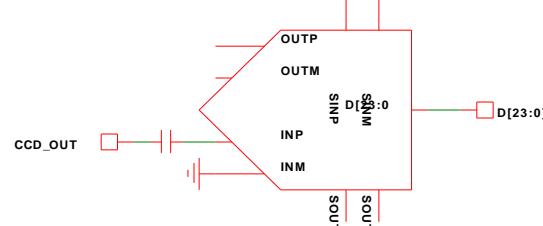


CCD Readout
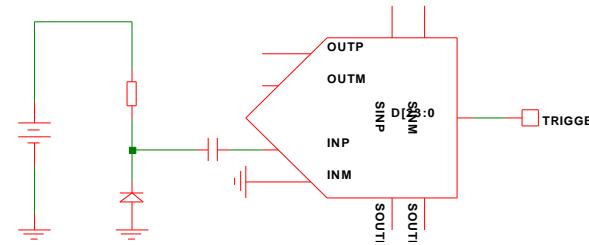
Radiation Detector

Radiation Spectrometer

ADC, DAC

Filter – Low pass/Semi-Gaussian Shaper

Amplifier – Voltage/Current/Charge – Single ended/Differential

## Development of MF and HF Configurable Instrumentation ASIC

Specification - Architecture
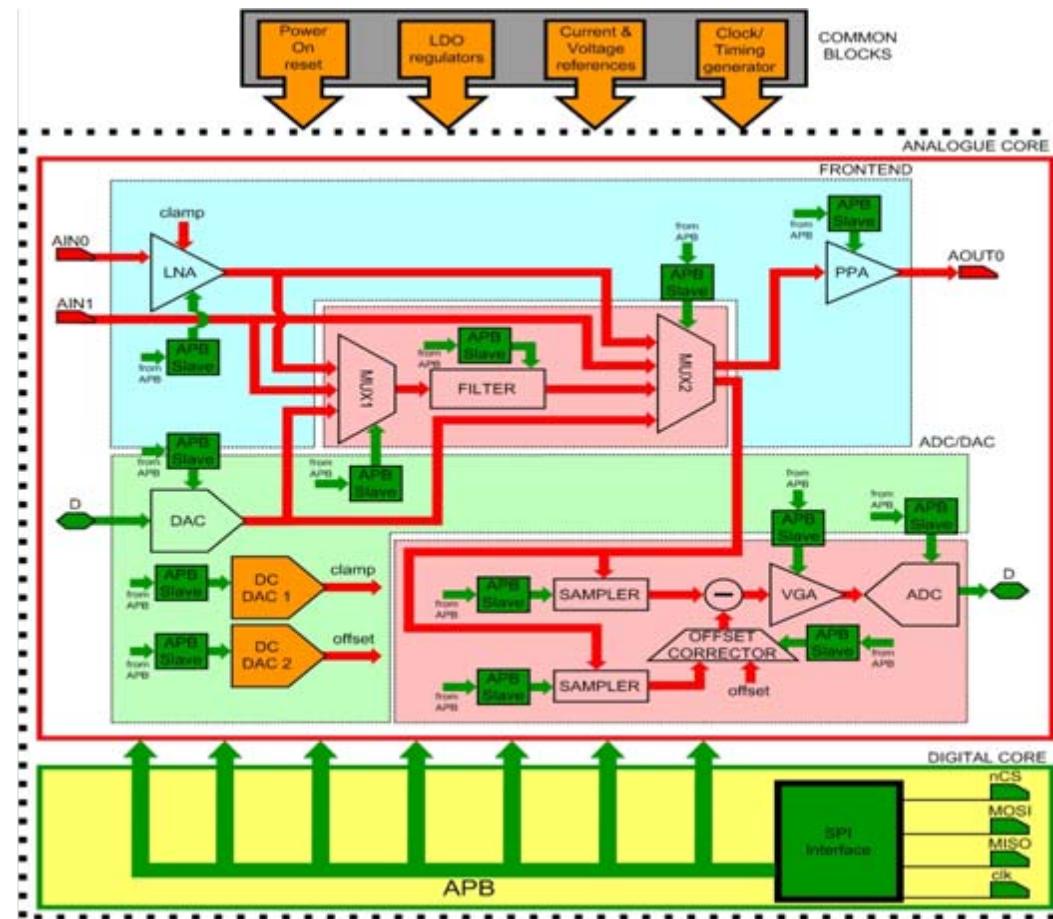
## Development of MF and HF Configurable Instrumentation ASIC

### CCD signal processor
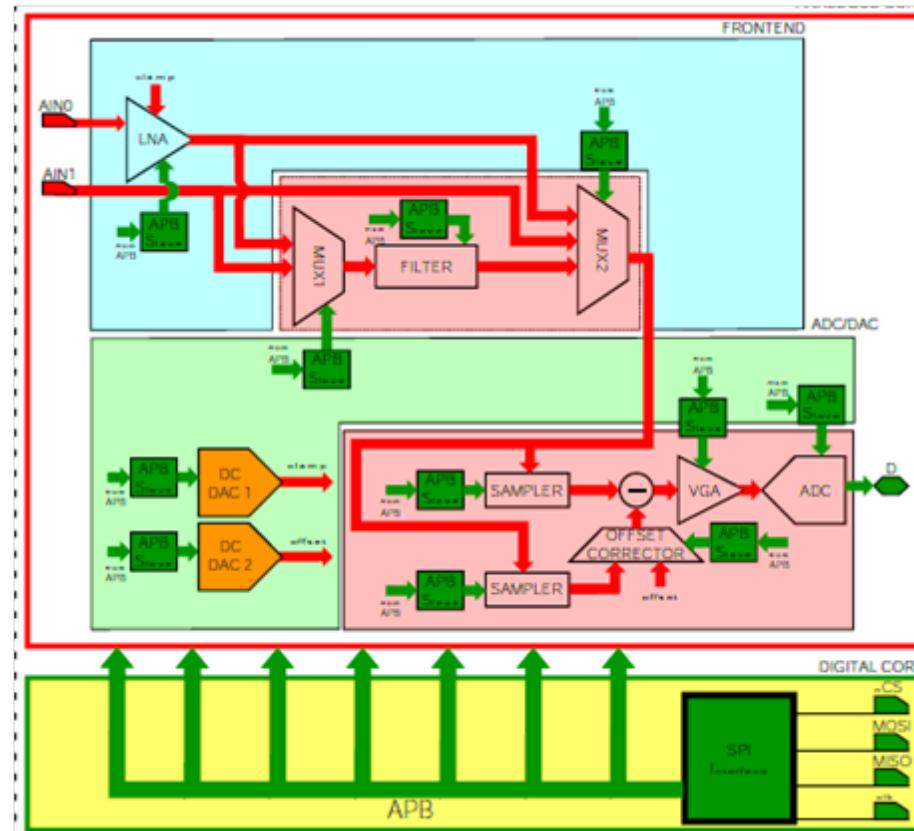
## Development of MF and HF Configurable Instrumentation ASIC

### CCD - signal processor

| Nº | Parameter | HF | MF | Unit |
|----|-----------|-----|-----|------|
| 1 | Input range | [0; 1.5] | [0; 1.5] | V |
| 2 | Input clamping | Configurable from 0 to 1.5 | Configurable from 0 to 1.5 | V |
| 3 | Input clamping step | 100 | 100 | mV |
| 4 | V/V gain (before filtering) | Configurable from -6 to 30 | Configurable from -6 to 30 | dB |
| 6 | V/V gain flatness | 0.4 | 0.4 | dB |
| 7 | Noise insertion (before filtering) | 5 | 5 | nV/√Hz |
| 8 | Offset correction (after filtering) | Configurable from 10m to 1 | Configurable from 10m to 1 | V |
| 9 | Offset correction step (after filtering) | 10m | 10m | mV |
| 10 | V/V gain (before conversion) | Configurable from 0 to 30 | Configurable from 0 to 30 | dB |
| 11 | Sample rate | Configurable from 10 to 100 | Configurable from 0.1 to 10 | MHz |
| 12 | Effective Nº of bits | 12@10 10@100 | 17@0.1 14@1 12@10 | Bits@MHz |
| 13 | ASIC current consumption | 200 | 27 | mA |

## Development of MF and HF Configurable Instrumentation ASIC

Radiation detector

Radiation spectrometer
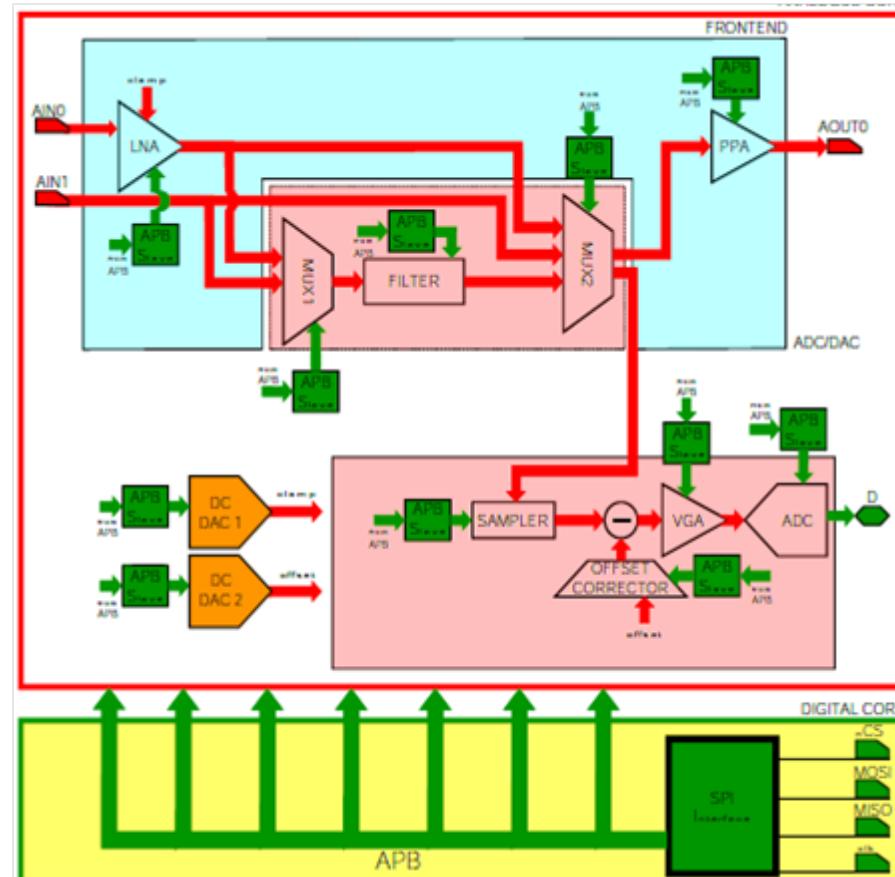
## Development of MF and HF Configurable Instrumentation ASIC

### Radiation detector

| Nº | Parameter | HF | MF | Unit |
|----|-----------|-----|-----|------|
| 1 | ENC | 50* | 80* | $e_{rms}$ |
| 2 | ENC slope | 5.0* | 1.6* | $e_{rms}$/pF |
| 3 | Range | 200@0.2pF 20000@20pF | 200@0.2pF 20000@20pF | fC |
| 4 | Peaking time for Gaussian shaper | [0.05; 1] | [0.1; 10] | µs |
| 5 | Peaking time accuracy for Gaussian shaper | 5 | 5 | % |
| 6 | Threshold level | [10; 1000] | [10; 1000] | mV |
| 7 | Threshold step | 10 | 10 | mV |
| 8 | Current consumption contribution of LNA and filter | 70 | 70 | mA |

## Development of MF and HF Configurable Instrumentation ASIC

## Radiation spectrometer

| Nº | Parameter | HF | MF | Unit |
|---|---|---|---|---|
| 1 | ENC | 50* | 80* | $e_{rms}$ |
| 2 | ENC slope | 5* | 1.6* | $e_{rms}/pF$ |
| 3 | Range | 200 @ 0.2pF<br>20000 @ 20pF | 200 @ 0.2pF<br>20000 @ 20pF | fC |
| 4 | Peaking time for Gaussian shaper | [0.1; 10] | [0.1; 10] | μs |
| 5 | Peaking time accuracy for Gaussian shaper | 5 | 5 | % |
| 6 | Effective number of bits | 12@10<br>10@100 | 17 @ 0.1<br>14 @ 1<br>12 @ 10 | bits@MHz |
| 7 | Threshold level | [10; 1000] | [10; 1000] | mV |
| 8 | Threshold step | 10 | 10 | mV |
| 9 | Current consumption contribution of LNA and filter | 200 | 4.5 | mA |

## Development of MF and HF Configurable Instrumentation ASIC

ADC
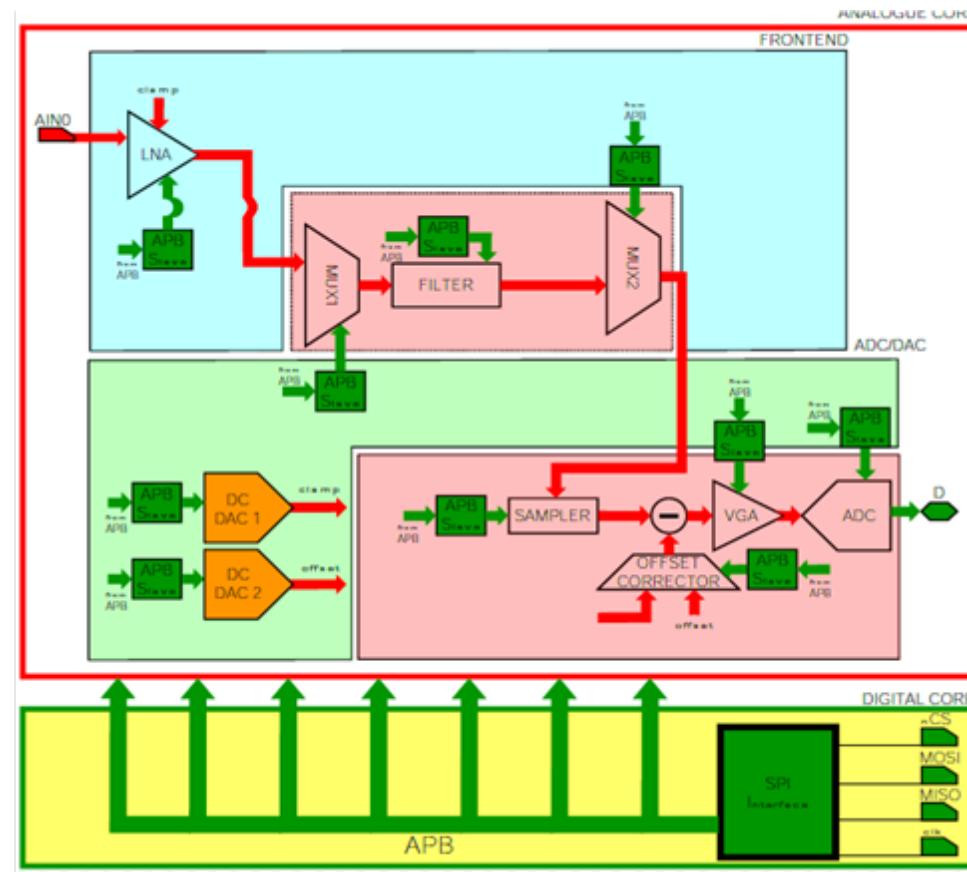
# Specification

## Development of MF and HF Configurable Instrumentation ASIC

### ADC

| No | Parameter | HF | MF | Unit |
|---|---|---|---|---|
| 1 | Number of bits | 15 @ 10<br>15 @ 100 | 19 @ 0.1<br>16 @ 1<br>14 @ 10 | Bits @ MHz |
| 2 | Sample rate | [10; 100] | [0.1; 10] | MHz |
| 3 | Effective number of bits | 12 @ 10<br>10 @ 100 | 17 @ 0.1<br>14 @ 1<br>12 @ 10 | Bits @ MHz |
| 4 | Input range | 2 | 2 | Vdpk |
| 5 | Maximum gain flatness | 0.2 | 0.2 | dB |
| 6 | Maximum gain stability | 0.1 | 0.1 | dB |
| 7 | Minimum THD | 74@10<br>64@100 | 104@0.1<br>84@1<br>74@10 | dB@MHz |
| 8 | Minimum SFDR | 74@ 10<br>64 @ 100 | 104 @ 0.1<br>84 @ 1<br>74 @ 10 | dB@ MHz |
| 9 | Current consumption contribution of ADC block | 250 @ 100 | 2 @ 0.1<br>4 @ 1<br>20 @ 10 | mA@MHz |

## Development of MF and HF Configurable Instrumentation ASIC

DAC
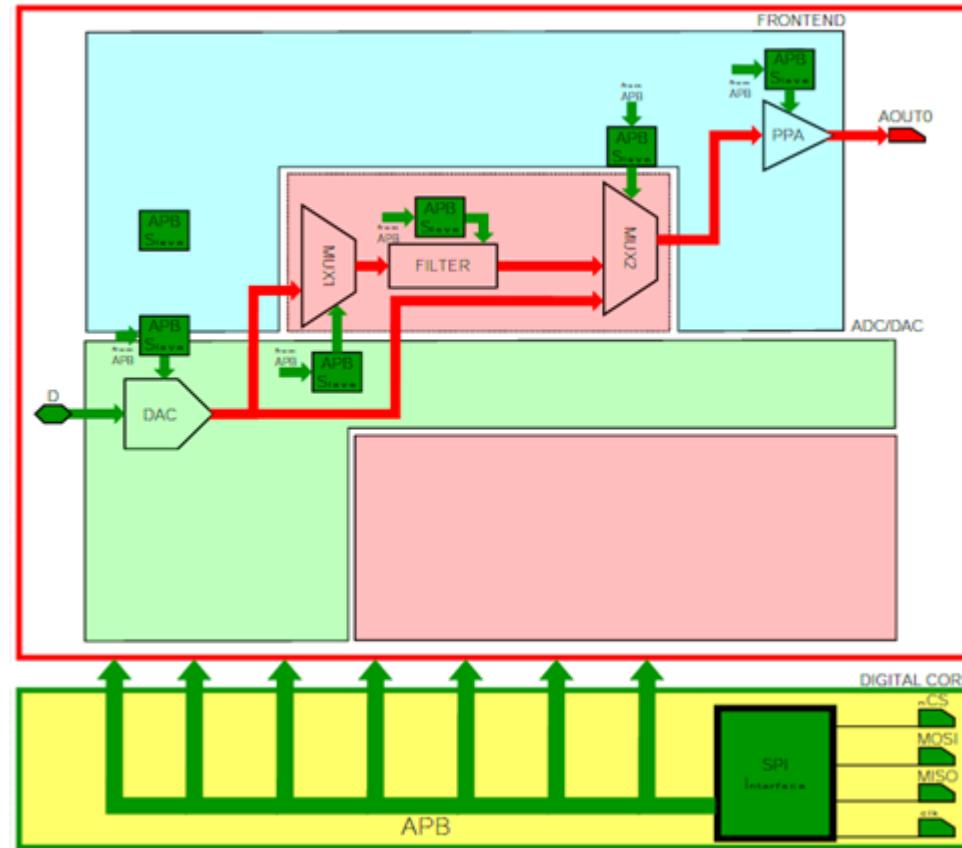
# Specification

## Development of MF and HF Configurable Instrumentation ASIC

### DAC

| Nº | Parameter | HF | MF | Unit |
|----|-----------|-----|-----|------|
| 1 | Number of bits | 15 @ 10<br>15 @ 100 | 19@0.1<br>16@1<br>14@10 | Bits @ MHz |
| 2 | Sample rate | [100] | [0.1; 10] | MHz |
| 3 | Effective number of bits | 12 @ 10<br>9 @ 100 | 17@0.1<br>14@1<br>12@10 | Bits @ MHz |
| 4 | Input range | 2 | 2 | Vdpk |
| 5 | Maximum gain flatness | 4 | 0.2 | dB |
| 6 | Maximum gain stability | 0.1 | 0.1 | dB |
| 7 | Minimum THD | 72@10<br>57@100 | 124@0.1<br>104@1<br>84@10 | dB@MHz |
| 8 | Minimum SFDR | 74 @ 10<br>59 @ 100 | 124 @ 0.1<br>104 @ 1<br>84 @ 10 | dB@ MHz |
| 9 | Current consumption contribution of DAC block | 60 @ 100 | 1 @ 0.1<br>2 @ 1<br>20 @ 10 | mA@MHz |

# History

KO - 17-09-2010

ADR - 29-06-2011

Consortium

| | | |
|---|---|---|
| 1. Arquimea – Madrid | System | |
| 2. CSIC (IMB-CNM) – Barcelona | MF ADC/DAC | |
| 3. CSIC (IMSE-CNM)– Seville | HF ADC/DAC | |
| 4. UPC - University of Catalunya – Barcelona | MF/HF Front-end | |
| 5. UC3M – University of Carlos III – Madrid | Digital | |

# Status

Circuit verification of ASIC blocks

- Low noise amplifier

- Output amplifier

- ADC - HF

- DAC – HF

- Common blocks : Bandgap – Current/Voltage reference generator

Circuit design of ASIC blocks

- ADC – MF

- DAC - MF

- Filter – MF/HF

- Sampler

# Plan

Project

    PDR – Q2 2012

    CDR – Q3 2012

Test vehicles

    Q3 2012 HF ASIC

    Q4 2012 MF ASIC

Radiation tests

    Q4 2012

Prototypes

    Q1 2013

# Review/Simulation - JUICE
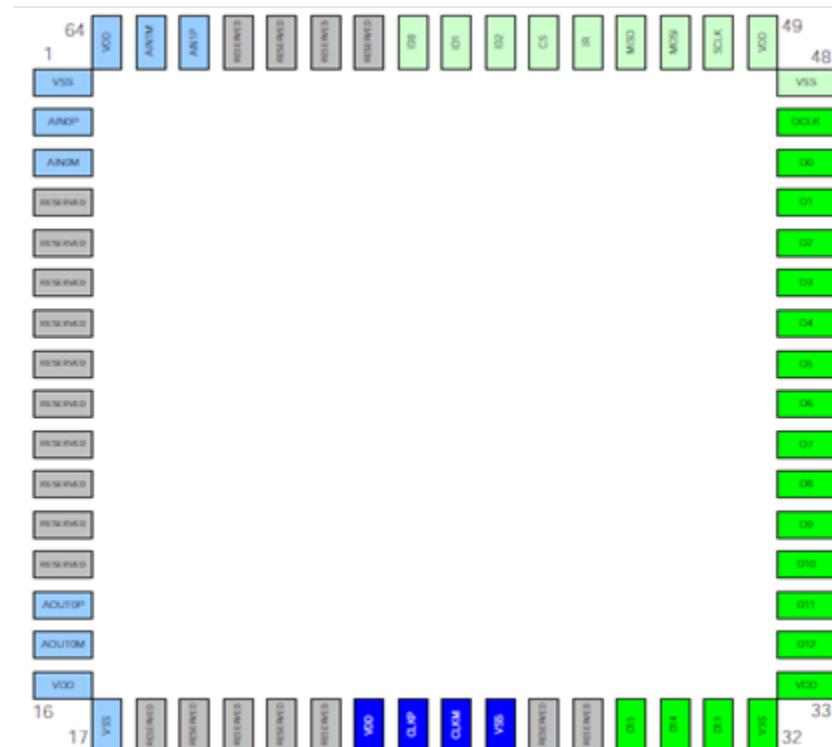
Performance specification review

    ASIC specification - available for review

Application review

    Model of ASIC developed (VerilogA) – available for simulation

    Applications covered

    1) ADC

    2) DAC

    3) Amplifier

    4) Filter

    5) Radiation detector

    6) Radiaton spectrometer

    7) CCD processor

# Review/Testing – JUICE

Performance specification

    Provide e-mail to ESA to obtain a copy


Application review

    Sign a NDA with Arquimea to obtain a copy

    Provide application feedback to ESA

    Demonstration of the Model at JUICE Instrument Workshop


Test-vehicle testing

    Inform ESA about the intention to participate in the testing

    Provide information on the test application

**THANK YOU**

Richard Jansen
TEC-EDM, ESTEC
Richard.Jansen@esa.int