MIXED SIGNAL RADIATION TOLERANT DESIGN WITH DARE

imec

OVERVIEW

- Mixed Signal ASIC Design Flow
- Design Analog Blocks
- Integration of Analog Blocks
- DARE ASICs
  - LEONDARE
  - KNUT
  - SSOC
- Conclusions

Design
Against
Radiation
Effects

DARE180
DARE+
(DARE90)

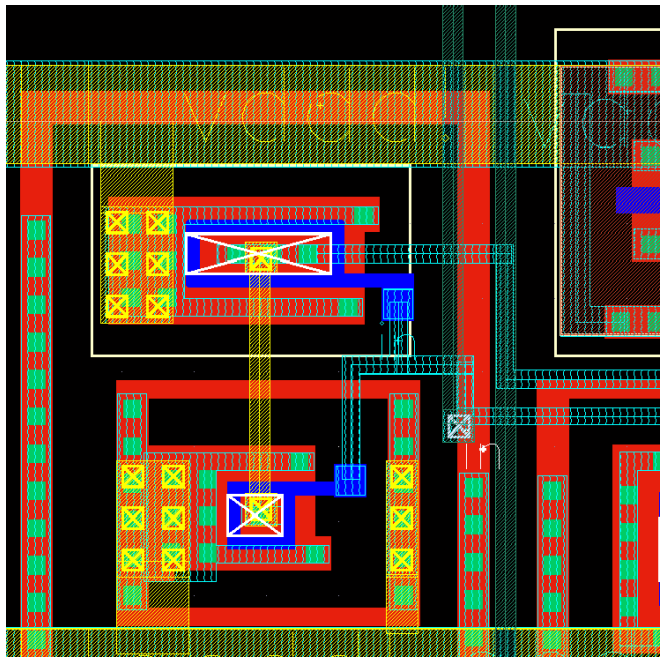
MIXED SIGNAL DESIGN FLOW

- Digital-on-top approach vs Analog-on-top depends on:
  - Complexity of digital part
  - Interface (# signals, timing) digital-analog
  - Area estimation digital/analog
  - Number/type of analog blocks
  - Experience/familiarity with digital/analog flow

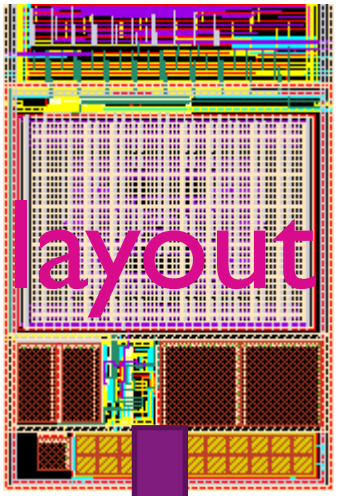
  $\Rightarrow$ digital-on-top preferred for DARE
- Extra requirements for analog blocks
  - Floor planning, placement and routing
    - Additional layers, additional labels, port placement, ..
  - Timing analysis
    - Additional simulations

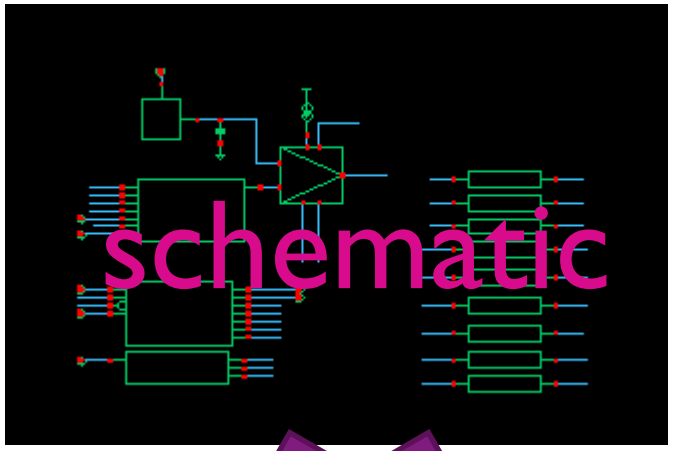
DESIGN ANALOG BLOCKS

- Schematic entry + SPICE simulation
- Standard available UMC Mixed-Mode PDK (IC6.1)
  - ⇒ Analog Design Kit enhancement for ELT and TID (DARE+)
- Standard DRC checking
- Custom LVS checking
- Extra RAD checking
  - ⇒ NMOS ELT compliance
  - ⇒ Presence of guard bands
  - ⇒ Forbidden polysilicon routing



INTEGRATION OF ANALOG BLOCKS

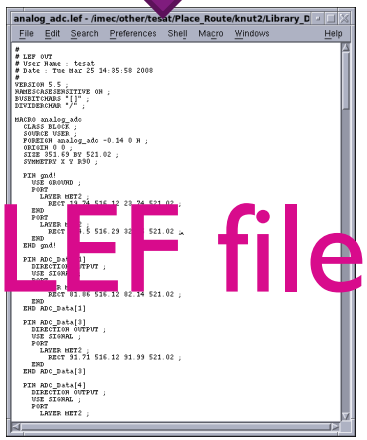


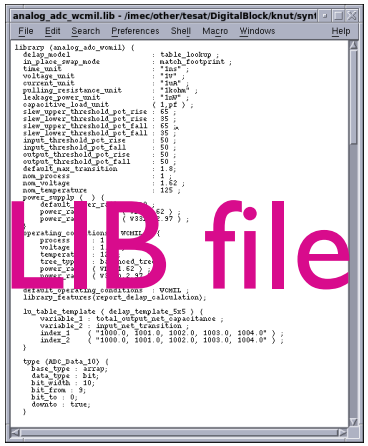


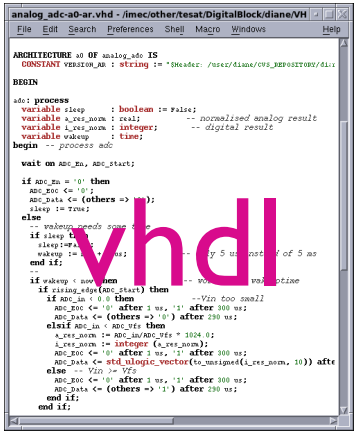
abstract generator
LEF script

analog simulation
LIB template

model description

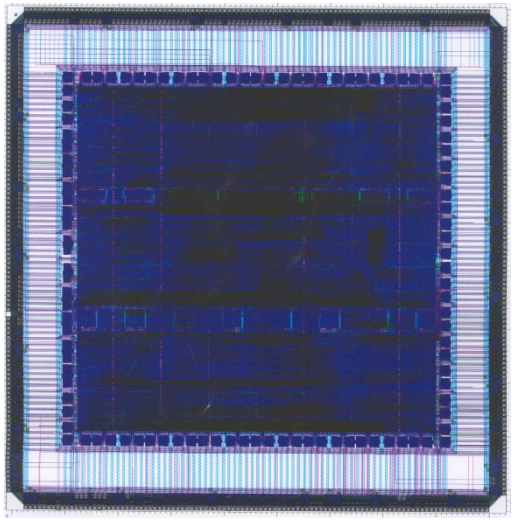




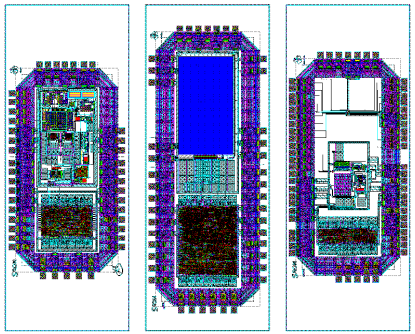


DARE ASICS: ESA PROJECTS

DROM

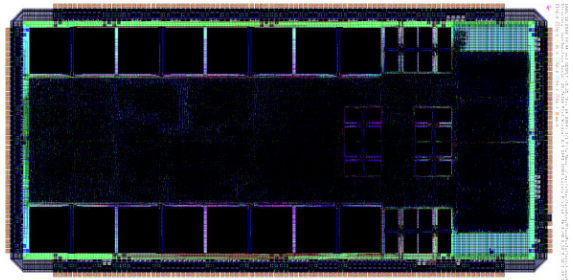


First functional DARE silicon

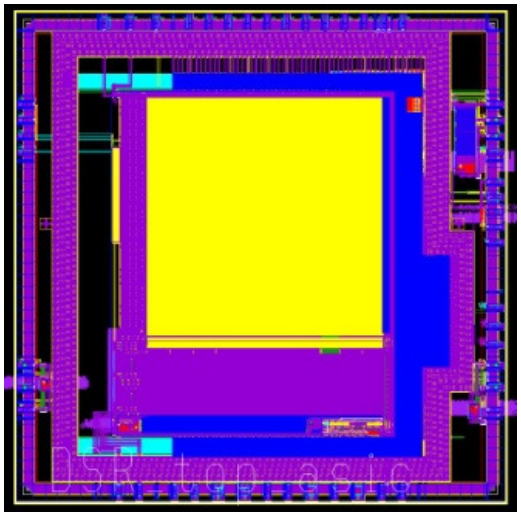


SRON Netherlands Institute for Space Research

LEONDARE

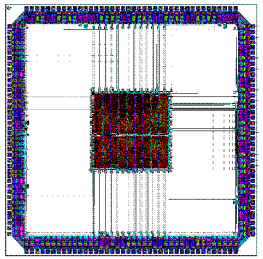


SSOC



CIS Port

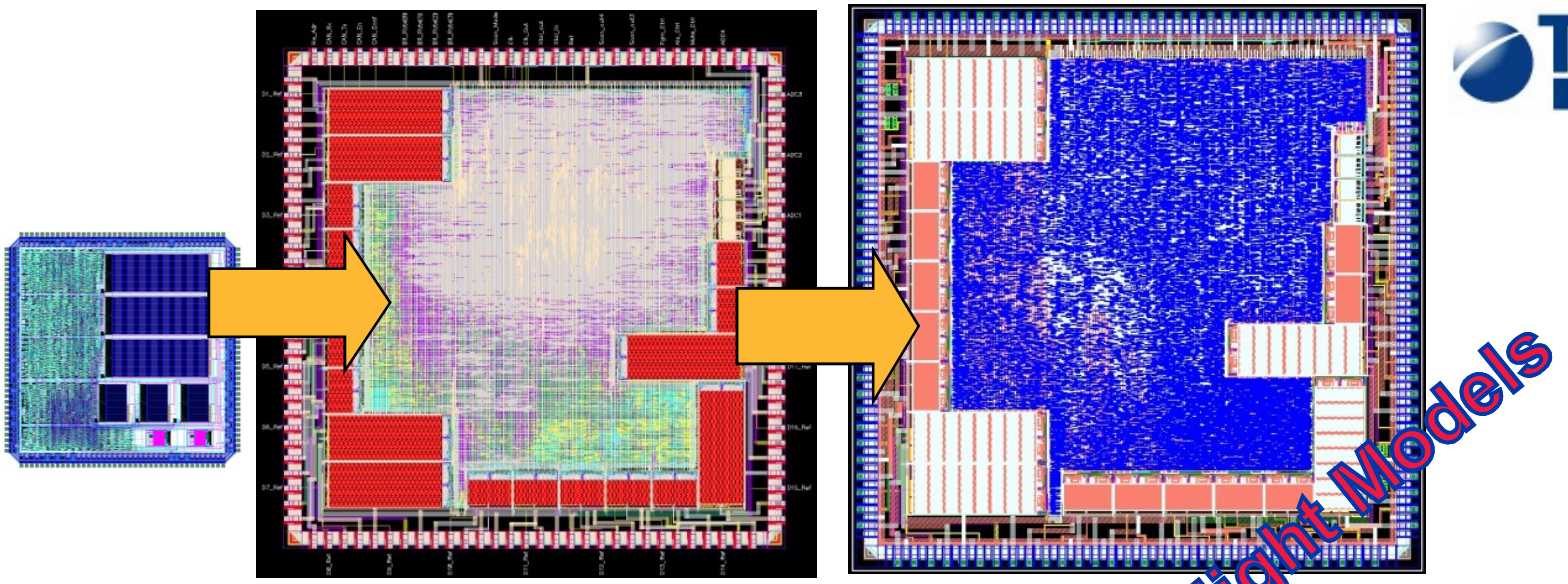
CMOSIS image sensors



RUAG

Muller-C gate added

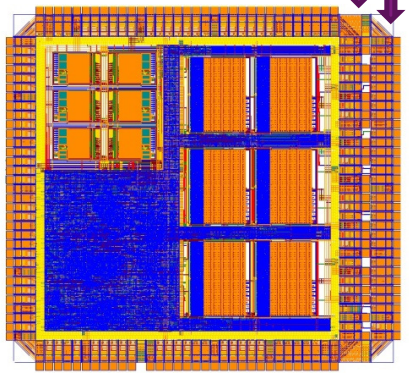
DARE ASICS: CUSTOMER CHIPS



TESAT SPACECOM

Flight Models

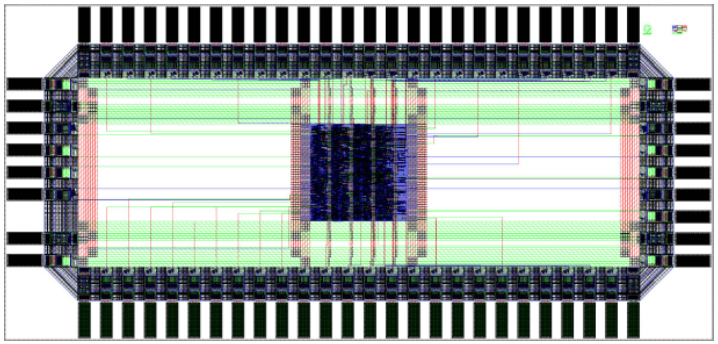
Dual bond



(Slow)
ADC & DAC
IP blocks

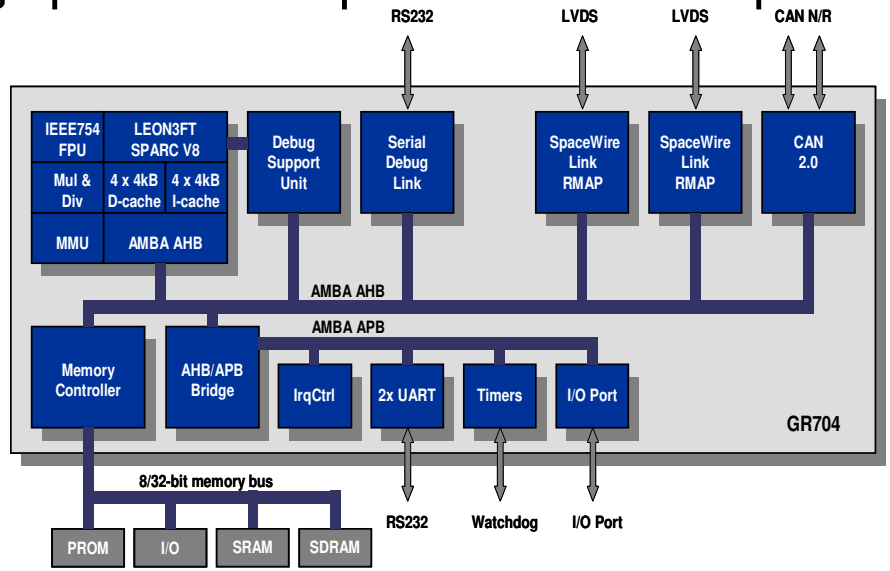
TESAT SPACECOM

ARQUIMEA



LEONDARE ASIC

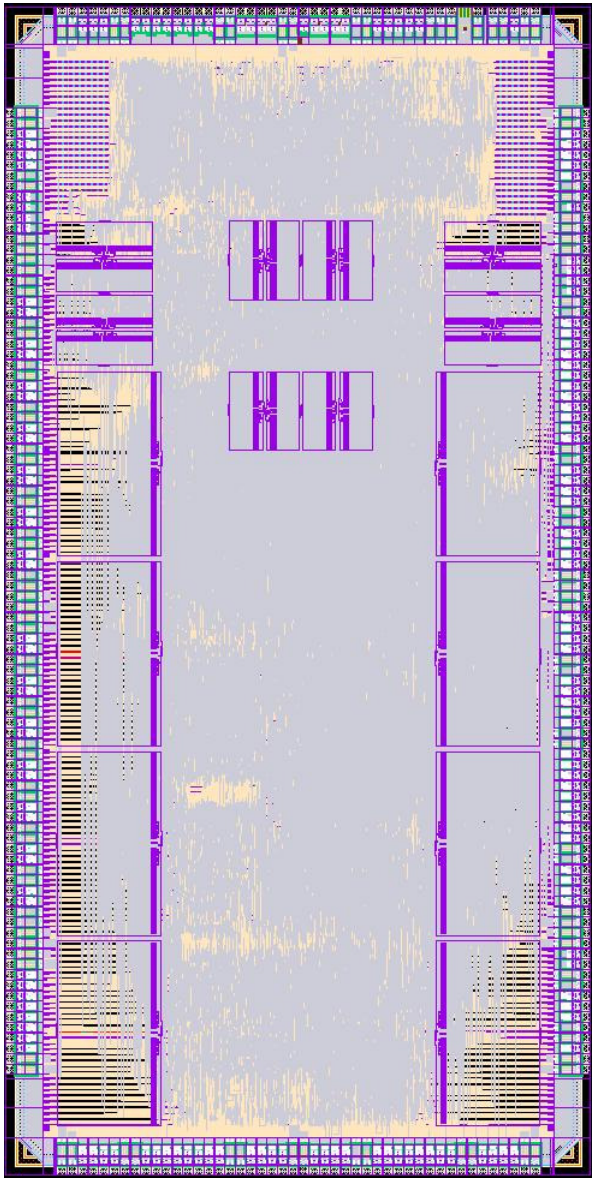
- Evaluate the technology according to a dedicated production and evaluation flow complying with the ESCC standards
- Aeroflex-Gaisler LEON3-FT IP + IP Peripherals
  - Appropriate complexity for evaluating a technology (SRAM, PLL, LVDS,…)
  - High-performance processor for the space domain



LEONDARE

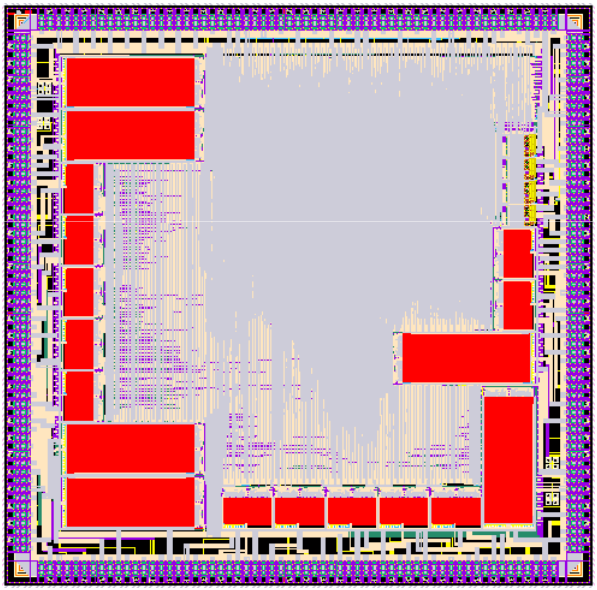
- 120 MHz
- PLL
- LVDS
- SRAM

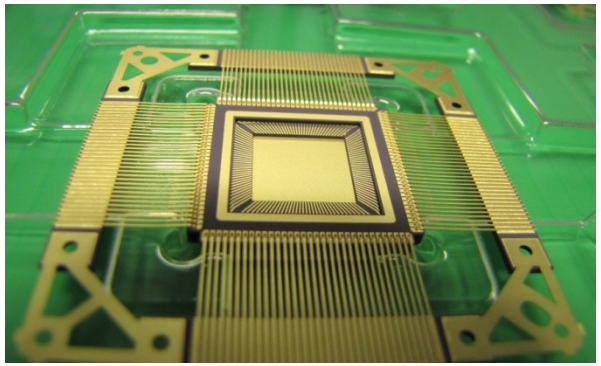
- CQFP256 (custom)
- Evaluation & Qualification



KNUT ASIC

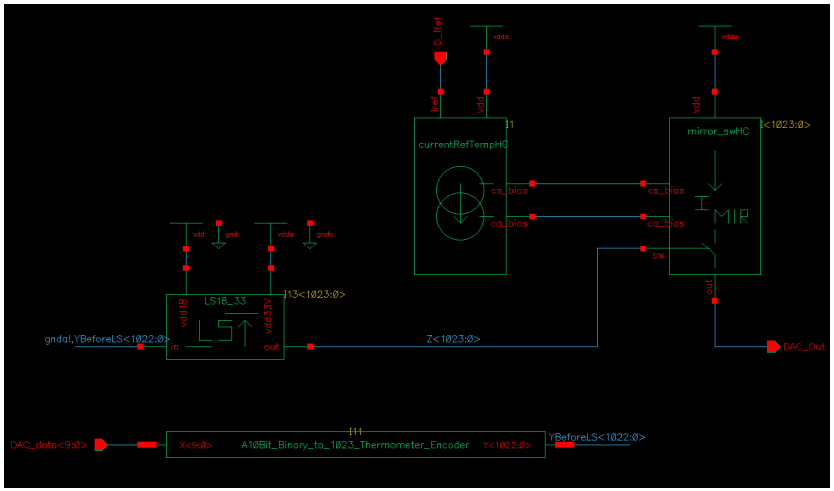
- TESAT Spacecom GmbH & Co.KG
- UMC 180nm 1P6M + MiM
- Mixed Signal ASIC
  - 88 mm^2
  - 120 I/O
  - Digital core 300K gates
  - Analog blocks ADC (4)
    DAC (18)
    I/O (88)

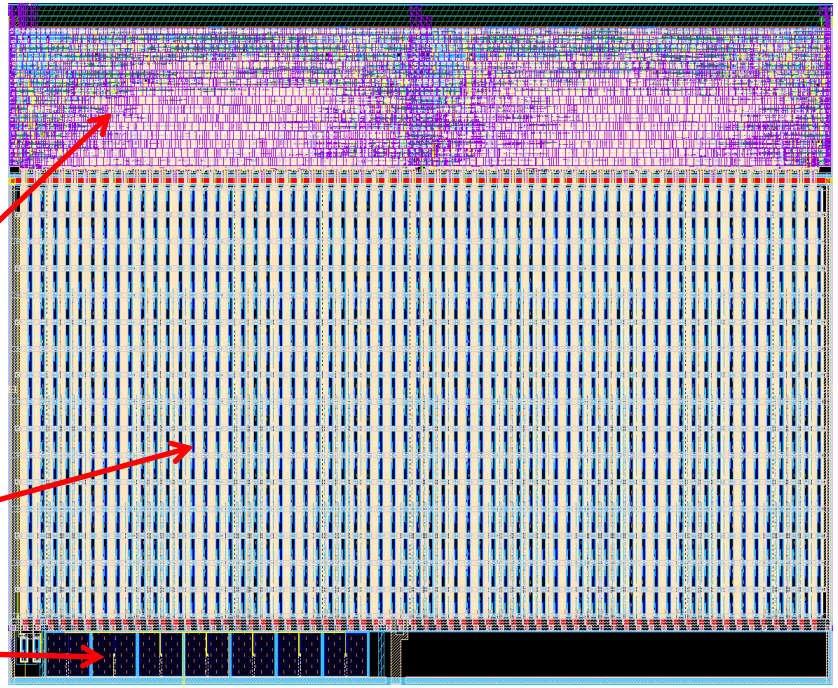




10 BIT DAC

Specification	Range
Resolution	10 bit
DNL	< 1 LSB
INL	< 1 LSB
Temperature Range	-55 °C .. +125 °C
Analog Supply Voltage	VDDA = 3.3 V +/- 10%
Temperature Drift	< 10 LSB
ILSB low current range	1 µA .. 6 µA
ILSB high current range	5 µA .. 30 µA
Total Dose	100 krad





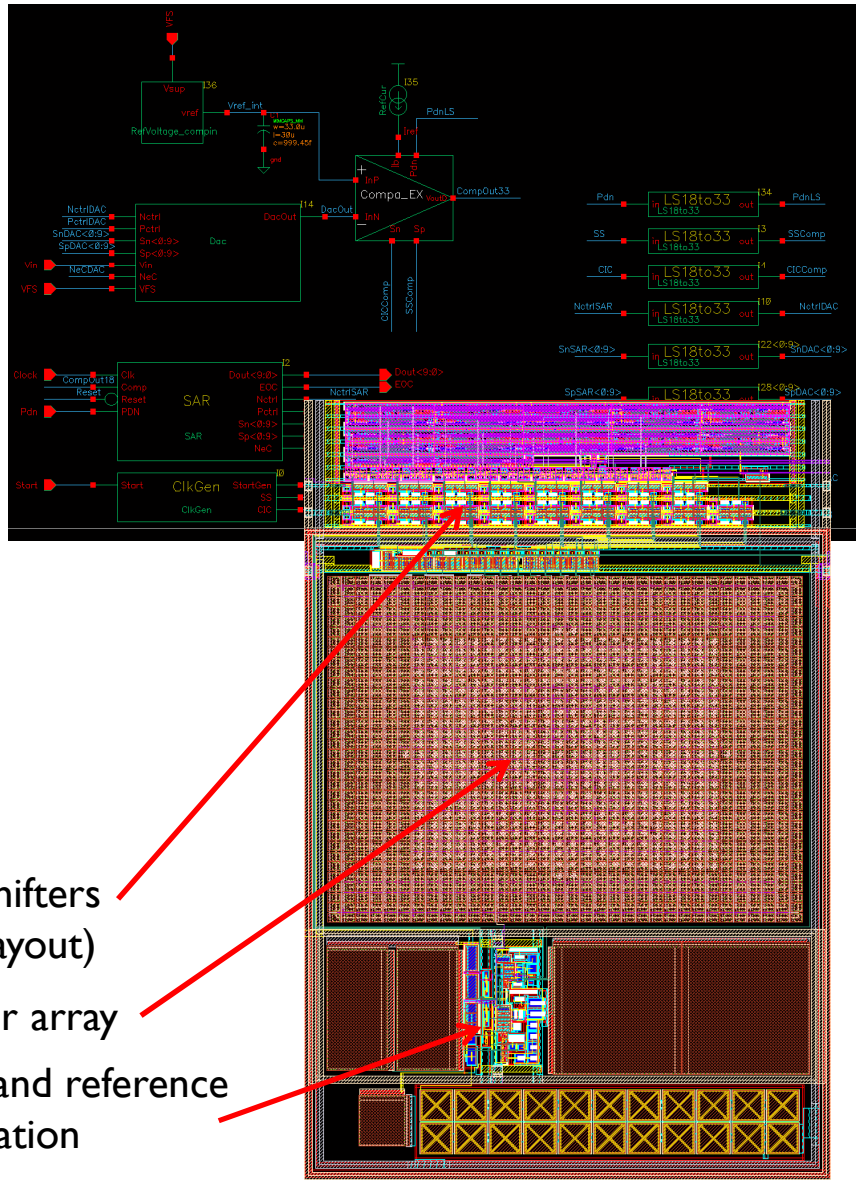
10b Bin2Thermo
(fully digital P&R)

Current sources with
local level shifter

Bias voltage generation

10 BIT ADC

Specification	Range
Resolution	10 bit
DNL	< 1 LSB
INL	< 1 LSB
Temperature Range	-55 °C .. +125 °C
Analog Supply Voltage	VDDA = 3.3 V +/- 10%
Temperature Drift	< 1 LSB
Input Voltage Range	0 < Vin < VFS
Full Scale Voltage	1.4 < VFS < VDDA
Conversion Speed	< 1 ms
Total Dose	100 krad

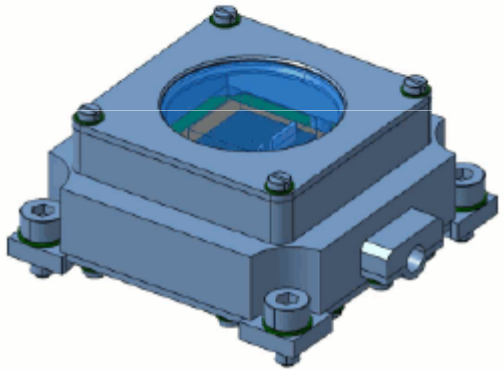


DIGITAL SUN SENSOR ON A CHIP

Application

- smart image sensor prototype
- accurate centroiding of sun image on 2D pixel array for spacecraft altitude determination
- autonomous, plug and play: light in – coordinates out

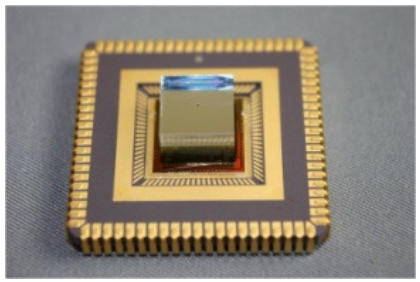
ESA contract 21835/08/NL/ST



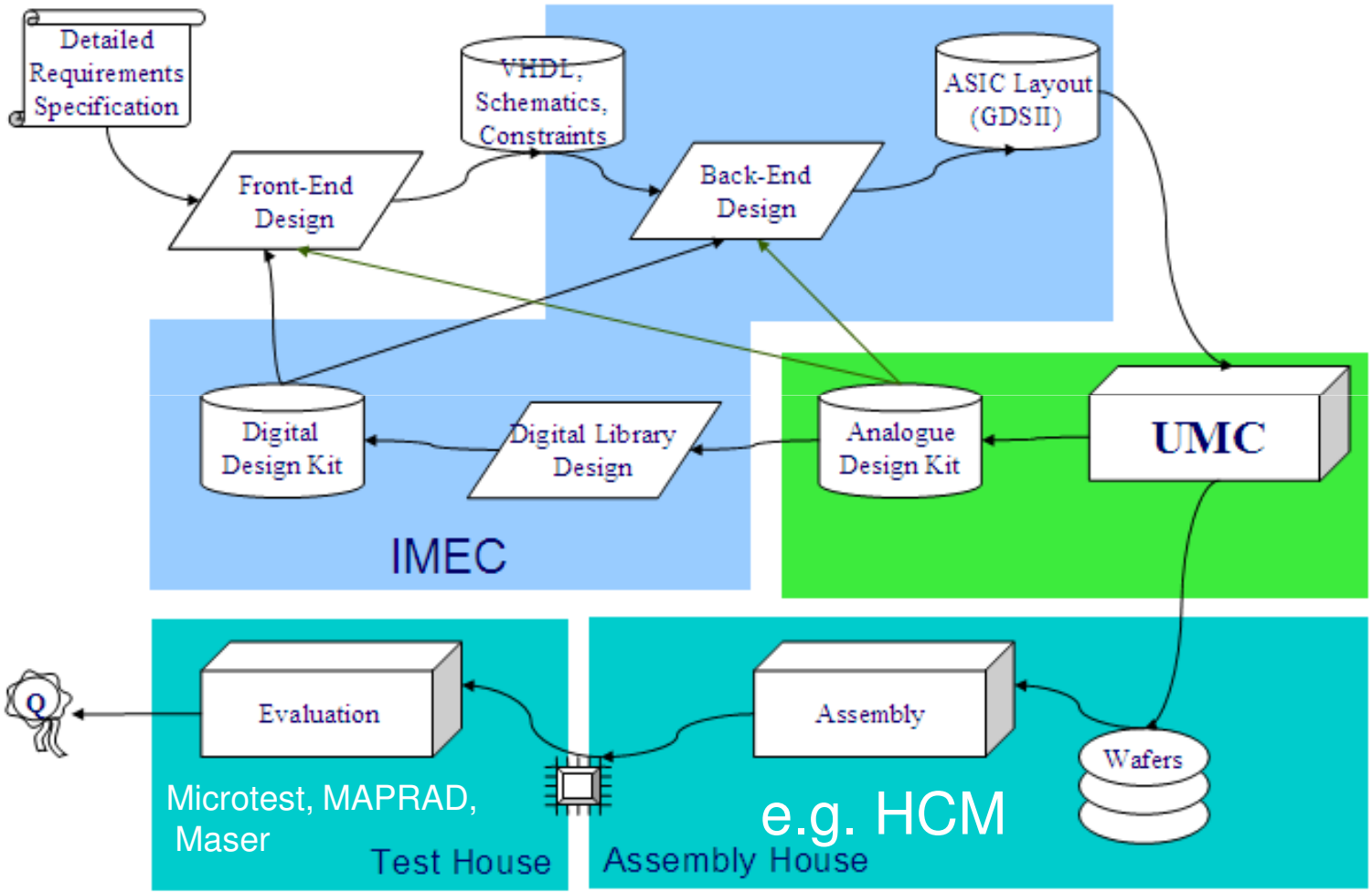
- Selex Galileo (I): prime, unit design and test
- BAE Systems (UK): immersed MEMS optics
- CMOSIS (B): sensor chip design and test
- Kick-off: February 2009 => first silicon: June 2010

Key requirements: dimensions, cost, robustness, performance

- radiation (> 300 krad, SEU/SEL-insensitive)
- ESD
- supply: 7V peak, low-power (<200mW at 5V)
- sun detection: no false positives, even in solar storm

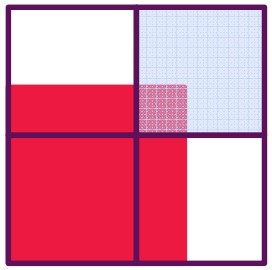


FROM SPECIFICATION TO FLIGHT MODELS

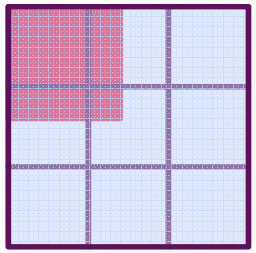


(UMC) PRODUCTION BUSINESS MODEL

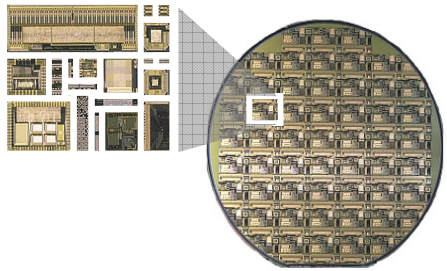
- MPW – scheduled runs
  - Square of 5x5mm^2 (1, 2, 4)
  - http://www.europractice-ic.com/docs/MPW2011-general-v7.pdf
  - EUR 16000/square
  - 40 dies guaranteed + 30/extra wafer (±1900 EUR/w)
  - Dice from WAT accepted wafers only/ no wafers



- Mini@sic – scheduled runs
  - After UMC approval for low cost access
  - EUR 2670/square (1525x1525 microns)
  - Amount of pins!



- Full Mask set – start any time
  - ±EUR 100k – can e.g. hold wafers before metal,...
  - Use ONLY this for Flight Models



CONCLUSIONS

- The feasibility of a Mixed Signal design flow for Space Applications with the DARE library is demonstrated for several ASICs
- The digital-on-top approach is preferred, but needs descriptions of the analog blocks for doing P&R, STA, IR-drop and power analysis
- RAD check gives added value in mixed-mode designs
- Analogue Design Kit: ELT and TID modeling upgrade under development

QUESTIONS ?

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Full Custom & Library Development: Geert.Thys@imec.be