Payload Data Processing Technologies for JUICE

JUICE instrument Workshop

ESOC, 9th -11th November 2011

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Presentation Overview

- Expected payload data processing requirements for JUICE
- Data compression technologies
- Data processing hardware: existing processors (Europe)
- Data processing hardware: recent ESA developments
- Data Processor Chip for Exploration Missions
- Summary and proposal for requirements consolidation

Expected Payload Data Processing Requirements

The following general requirements are expected for the processing of payload / instrument data:

Software
- Mix of signal processing and control code / general purpose processing
- Resource efficient and performant data compression
- re-use of established standards and qualified algorithms / software where possible

Hardware
- Sufficient processing performance (# MIPS)
- Radiation hardness at least some 100 krad, better 1 Mrad (=> DARE180)
- Sufficient reliability
- Very high power efficiency (Jupiter orbit => low solar power levels)
- Compatibility with established development flows and existing / qualified software

=> A demanding mixture !

Data Compression Technologies

Data compression is essential to reduce:
- on-board storage needs (saves mass, volume, power, cost)
- telemetry bandwidth needs (saves power = mass)

Data compression allows to do more science with less resources

Tradeoff lossy versus lossless compression required for each data source

Best (overall !) compression method may NOT provide best compression rate
- Optimal compression often needs excessive processing resources (memory, MIPS)
- Balanced performance/resource consumption is important
- CCSDS standardized compression algorithms have good compression performance at low implementation complexity
- Standardized algorithms are often already available in software toolbox of industry: lower cost, lower risk, higher maturity (software TRL)

Data compression should be used not only for science but also for HK data
- Typically for science data lossy compression is used (max science per data volume)
- For HK data lossless data compression is required

CCSDS & ESA Data Compression Algorithms

CCSDS algorithms

- Lossless (RICE) data compression (CCSDS 122.0-B-1)
- Lossless image compression (CCSDS 121.0-B-1)
- Lossy image compression (CCSDS 121.0-B-1)

Near-future CCSDS algorithms

- Lossless multispectral data compression (under standardization)
- Lossy multispectral data compression (under standardization)

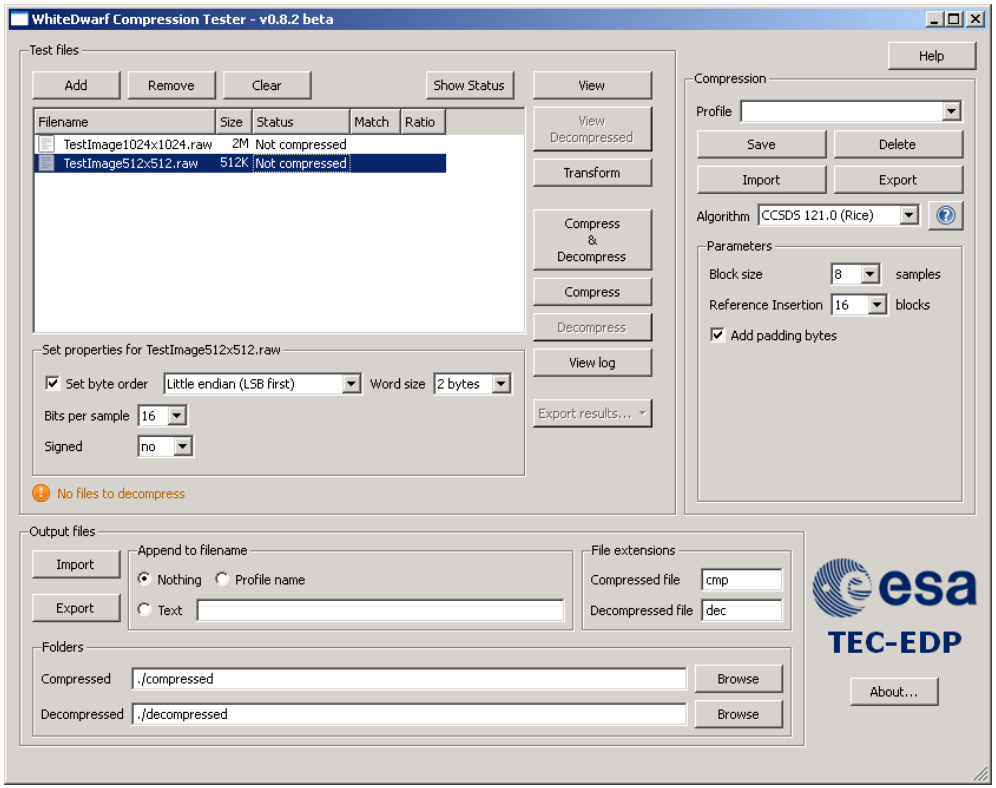
Algorithms developed with ESA support / ESA licensable

- Lossy multispectral data compression (available, use planned on ExoMars)

Various pre-processing algorithms

- Can increase compressibility of data by re-ordering etc.

ESA's Data Compression Evaluation Tool: WhiteDwarf



- Allows users to test recommended compression algorithms
- CCSDS standardized algorithms included, more to be added in future (multispectral image compression, etc)
- Supports both compression + decompression for easy verification
- Several data pre-processing methods are also implemented
- Application is both WIN and Linux based, executable, for distribution to the teams / industry: to be used for tests with user data
- Teams / industry can play with processing and compression algorithms and their parameters, select pre-processing steps, compression algorithm and best settings for their type of data

WhiteDwarf is available to ESA supported projects via:

http://www.esa.int/TEC/OBDP/SEM069KOXDG_0.html

Data Processing Hardware: Existing Processors (Europe)

The following processors are available in Europe:

Processor	**LEON2 & derivatives AT697F etc**	**LEON3 GR712RC**
Manufacturer / Technology	ATMEL 180nm	Aeroflex Gaisler Tower Semic. 180nm
Performance (max)	86MIPS, 23 MFLOPS	300 DMIPS, 200 MFLOPS
Clock	100 MHz max	125 MHz max
Radiation hardness SEU sensitivity (ca.)	300 krad (Si) tested < 10^-5/device/day	300 krad(Si) < 10^-6/device/dat
Architecture	Single core GPP	Dual core GPP
Power consumption	1W @ 100 MHz	1.5 W (?)

Mid-term (possibly): Quad core LEON (under development)

- All these processors are General Purpose Processors (GPP)
- Good at control processing, NOT good (=fast/power efficient) at signal processing
- radiation hardness acceptable ? TBC

Data Processing Hardware: Recent ESA Developments

General Purpose Processors:

- LEON 2 based devices are mainstream
- Quad-core LEON is under development:
    - based on new STM 65nm (radiation properties TBD)
    - high performance for GPP applications
    - real time application issues under investigation

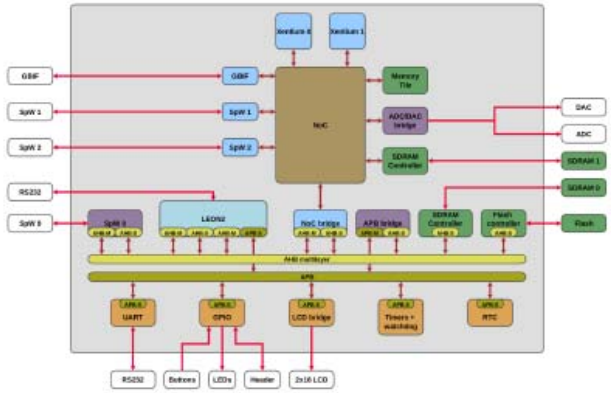
Signal Processors:

- Analog Devices based DSP (TSC21020) still used but outdated
- Next Generation European DSP IP evaluation / pre-selection ongoing
    - but: funding for next steps not clear
    - based on new STM 65nm (radiation properties TBD)

- Massively Parallel Processor Breadboarding study
    - Multicore fixed point DSP system, high performance, power efficient
    - single LEON control processor
    - Network-on-chip based, scalable, high on-chip bandwidth

Massively Parallel Processor Breadboarding (MPPB) Study

- TRP study, RECORE Systems, NL, 2009 – 2011
- Scalable high performance multicore architecture
- GPP + fixed-point DSPs + NoC
- FPGA based prototype, LEON2 + 2 DSP cores
- Goal is demonstration of key system aspects



Original requirements:

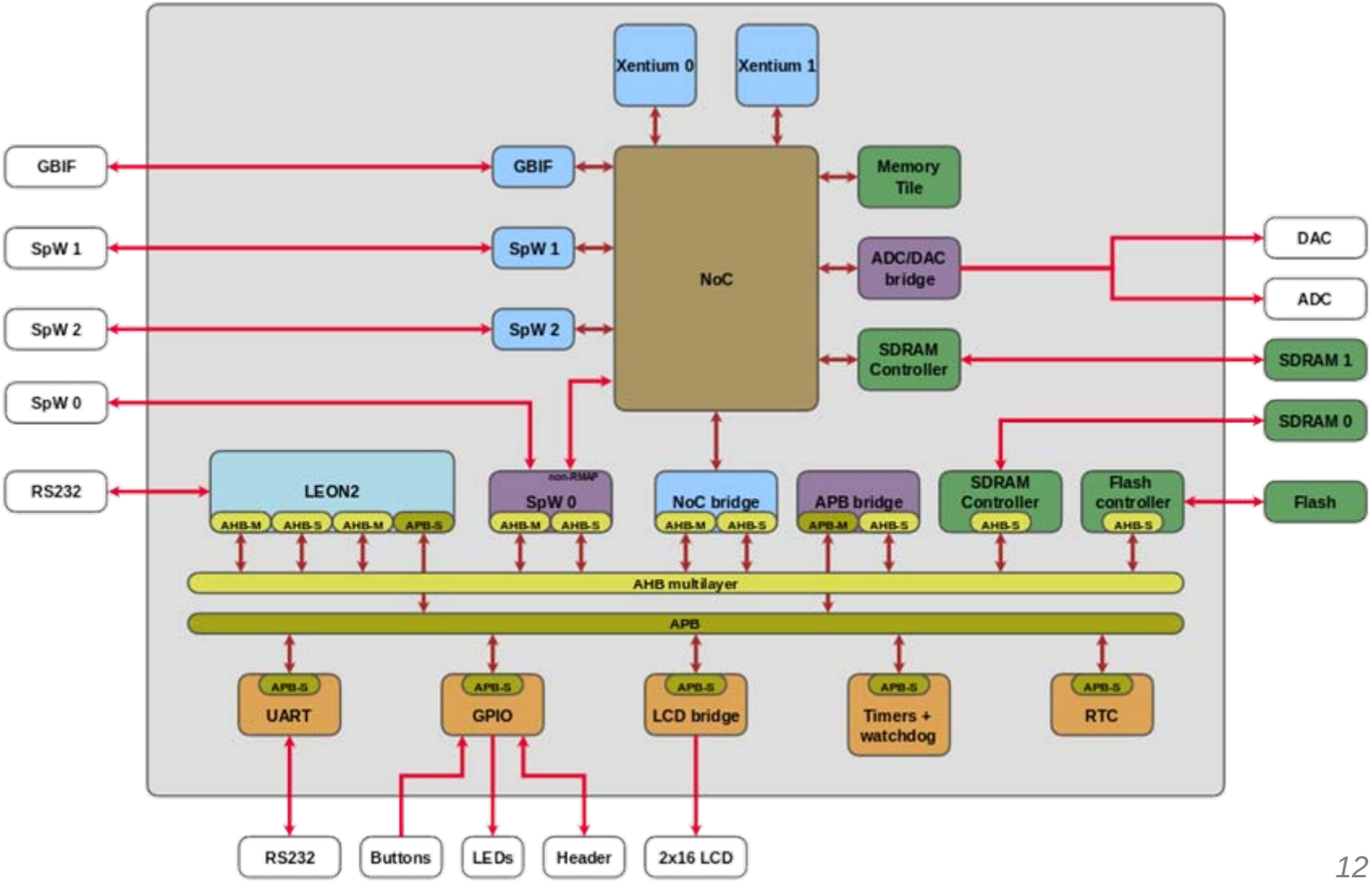
- **1 GFLOP achievable on space ASIC platform**
- **High scalability (up to dozens of DSP cores)**
- **low power consumption of space ASIC platform**
- **Space standard interfaces (SpW), ADC / DAC**
- **SDE, high level (C) programmable, assembler programmable**
- **FPGA based breadboard, DSP SDE, SEE hardening analysis, benchmark software**

MPPB demonstrator hardware

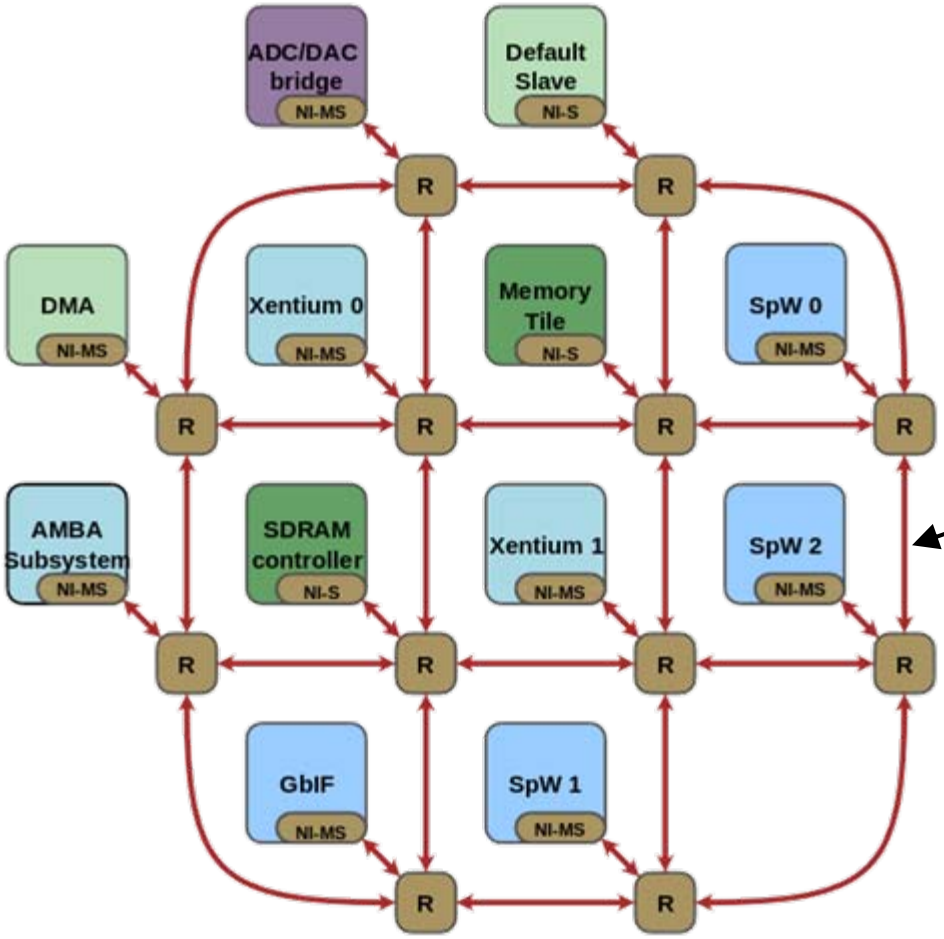
MPPB breadboard / demonstrator

- 50 MHz system clock
- 2 Xentium DSP tiles (@ 50MHz)
  - 400 16-bit MMAC/s
  - 200 32-bit MMAC/s
  - 200 16-bit complex MMAC/s
  - 64 KB data memory
  - 16 KB instruction cache
- 1 Leon2 processor (@ 50MHz)
  - 32-bit SPARC V8
  - Debug Support Unit / UART
- Network-on-Chip (@ 50MHz)
  - 32-bit packet-switched
  - 1.6 Gbps per link
    - In each direction
- Memories
  - 256 KB memory tile on NoC
  - 256 MB SDRAM on NoC
  - 256 MB SDRAM on AHB
  - 128 MB Flash on AHB
- SpaceWire (100 Mbps link)
  - 2 SpW-NoC interfaces
  - 1 RMAP-target interface
- Gigabit interface
  - 1.1 Gbps full-duplex
    - Aurora link layer protocol
- ADC/DAC-NoC interface
  - Configurable sampling rate
  - 14-bit, 40 MS/s AD6644
  - 12-bit, 40 MS/s DAC5662

MPPB architecture



Network on chip subsystem

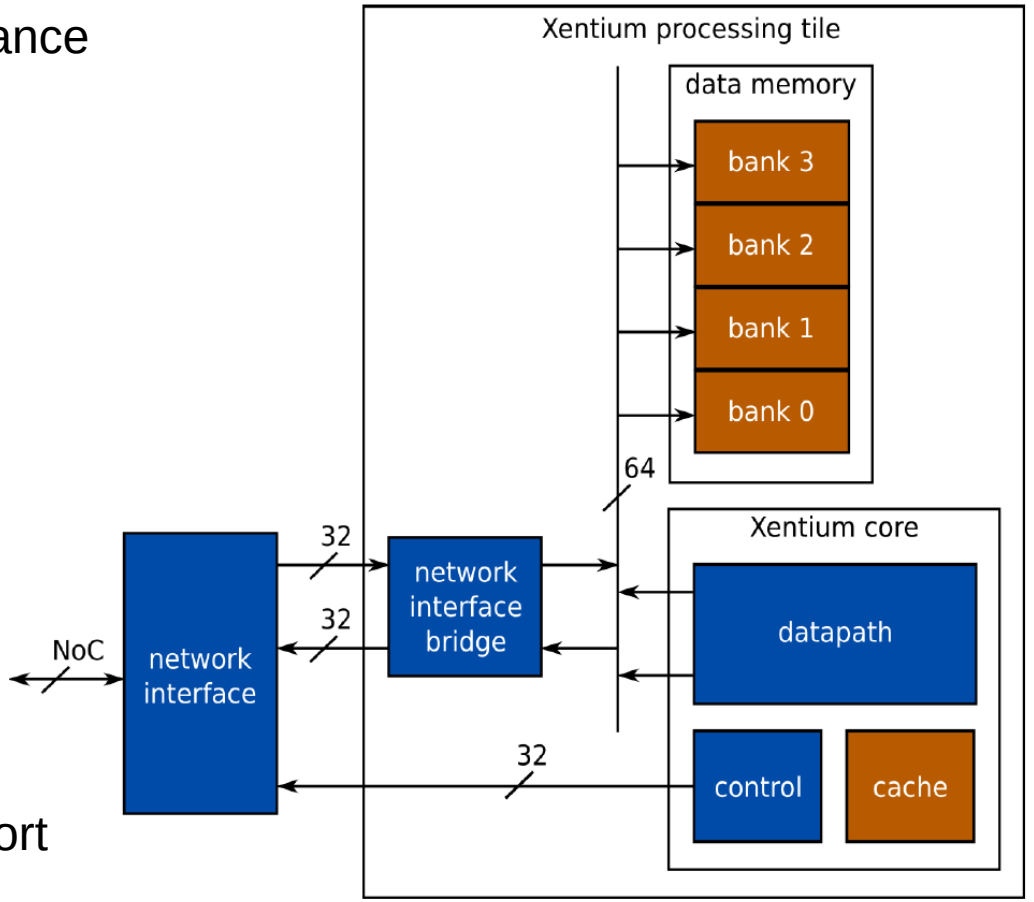


Network on chip lanes

- 32 bit parallel
- bi-directional
- full clock frequency
- 1.6 Gbit/sec @ 50 MHz
- 3.2 Gbit/sec @ 100 MHz

Xentium ® processing tile (fixed point VLIW DSP)

- Programmable high-performance fixed-point DSP core
- VLIW architecture with 10 parallel execution units
  - 4 16-bit MACs per cycle
  - 2 32-bit MACs per cycle
  - 2 16-bit complex MACs per cycle
- Data precision
  - 32/40-bit datapath
  - Block floating-point support



MPPB SW Development & Benchmarking

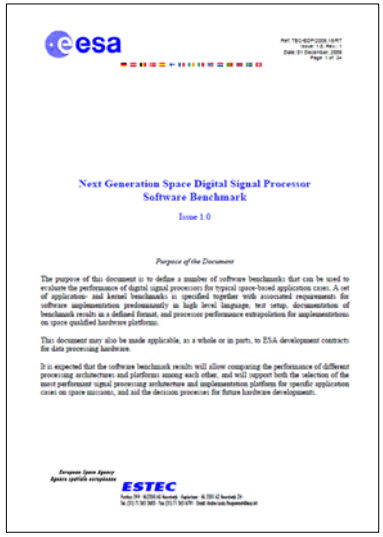
Benchmark Specification for MPPB

Based on the need identified at ADCSS07, ESA has defined an application oriented benchmark specification for payload data processing:

"Next Generation Space Digital Signal Processor Software Benchmark", TEC-EDP 2008/018/RT, available via email to SpaceDSP.benchmark@esa.int

Included:

- **I/O bandwidth**
- **Digital filters (FIR, various numbers of taps)**
- **FFT (1024pt, 2048pt, 4096 pt, 1920 pt)**
- **CCSDS lossless (RICE) data compression**
- **CCSDS lossless image data compression**
- **CCSDS lossy image data compression**
- **Kernel & application benchmarks**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Next Generation Space Digital Signal Processor Software Benchmark

Issue 1.0

Purpose of the Document

The purpose of this document is to define a number of software benchmarks that can be used to evaluate the performance of digital signal processors for typical space-based application cases. A set of application- and kernel benchmarks is specified together with associated requirements for software implementation, predominantly in high level language, test setup, documentation of benchmark results in a defined format, and processor performance extrapolation for implementations on space qualified hardware platforms.

This document may also be made applicable, as a whole or in part, to ESA development contracts for data processing hardware.

It is expected that the software benchmark results will allow comparing the performance of different processing architectures and platforms among each other, and will support both the selection of the most performant signal processing architecture and implementation platform for specific application cases on space missions, and aid the decision processes for future hardware development.

European Space Agency
Agence spatiale européenne

ESTEC

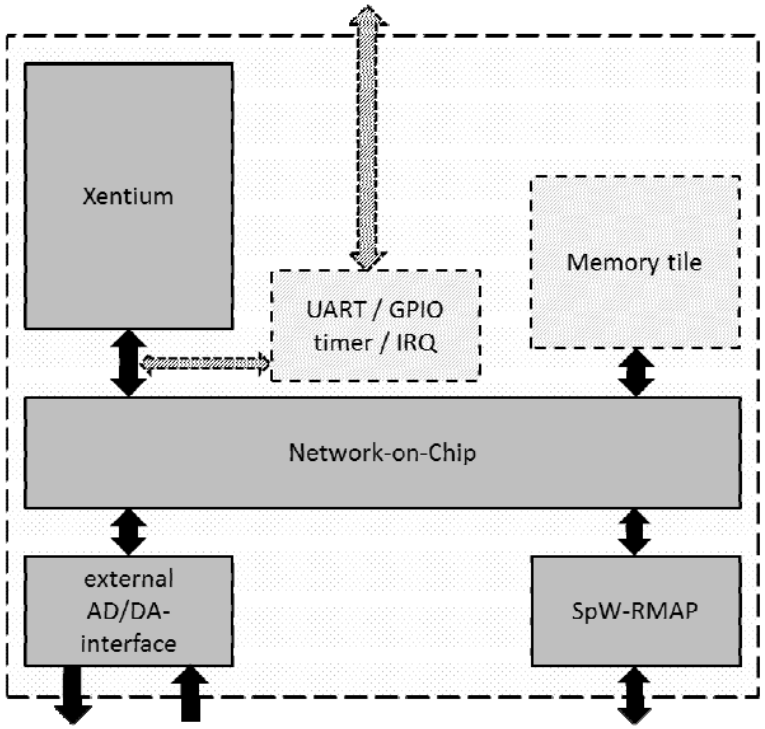
⇒ Many kernels and algorithms needed by payloads are already developed

⇒ Can be re-used in instrument on-board software

MPPB prototyping on DARE180 in DARE+

Key elements of MPPB architecture will be prototyped in DARE+:

- Xentium ® fixed-point DSP @ ca 125 MHz
- NoC (Network on Chip) routers and bridges
- NoC connected SpW with RMAP support
- NoC connected Memory Tile
- bridge to external ADC (STM RH1401)*
- bridge to external DAC (ADI AD768)*
- UART/I2C/SPI interface to external chips



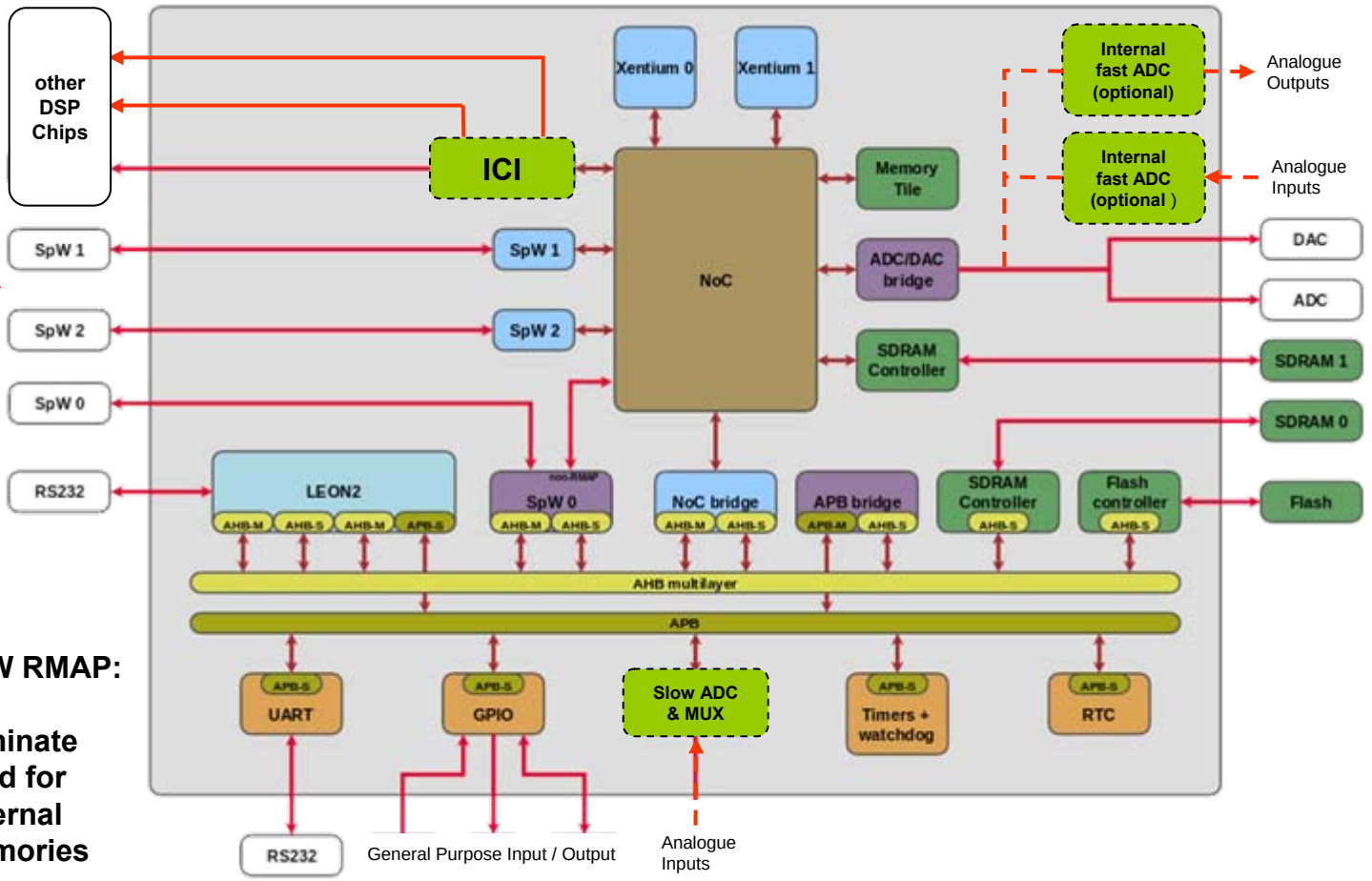
Other useful prototyping:

- analogue multiplexer elements

*interface compatibility to parallel DARE180 based ADC/DAC developments is goal

Data Processor Chip for Exploration Missions

Proposed architecture based on MPPB, to be tailored to JUICE needs



- **Additional optional elements added**

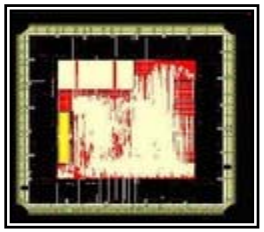
optional

- **other element IP is already developed and validated on FPGA**
- **NoC, bridges and DSPs demonstration in DARE+**

SpW RMAP: can eliminate need for external memories

Data Processor Chip for Exploration Missions

Early estimate of chip size in DARE180 ASIC Technology



Chip area
DARE180

Element	Minimum AD&DA bridges	HK ADC slow ADC & bridges	High speed AD & DA
LEON2 processor	9.00	9.00	9.00
Xentium DSP #1	24.00	24.00	24.00
Xentium DSP #2	24.00	24.00	24.00
Memory Tile 64 kbyte	17.00	17.00	17.00
4 x SpW	24.00	24.00	24.00
GPIO/UART	1.50	1.50	1.50
ADC/DAC bridges for ext converters	4.60	4.60	
NoC	3.60	3.60	3.60
low speed ADC+multiplexer		0.20	
High speed ADC			7.00
High speed DAC			2.00
Subtotal without margin & pads/rings/saw lanes	107.70	107.90	112.10
Margin 30% (P&R, pad ring, power ring, saw lanes)	32.31	32.37	33.63
Total chip area incl. margin	140.01	140.27	145.73
min square area	11.83	11.84	12.07

Performances: 1 Mrad, max DSP clock ca. 125 MHz => max ca > 1 Giga-Ops per sec

Chip die size ~12x12mm => suitable packages exist:: CQFP, CCGAm, etc

Data Processor Chip for Exploration Missions

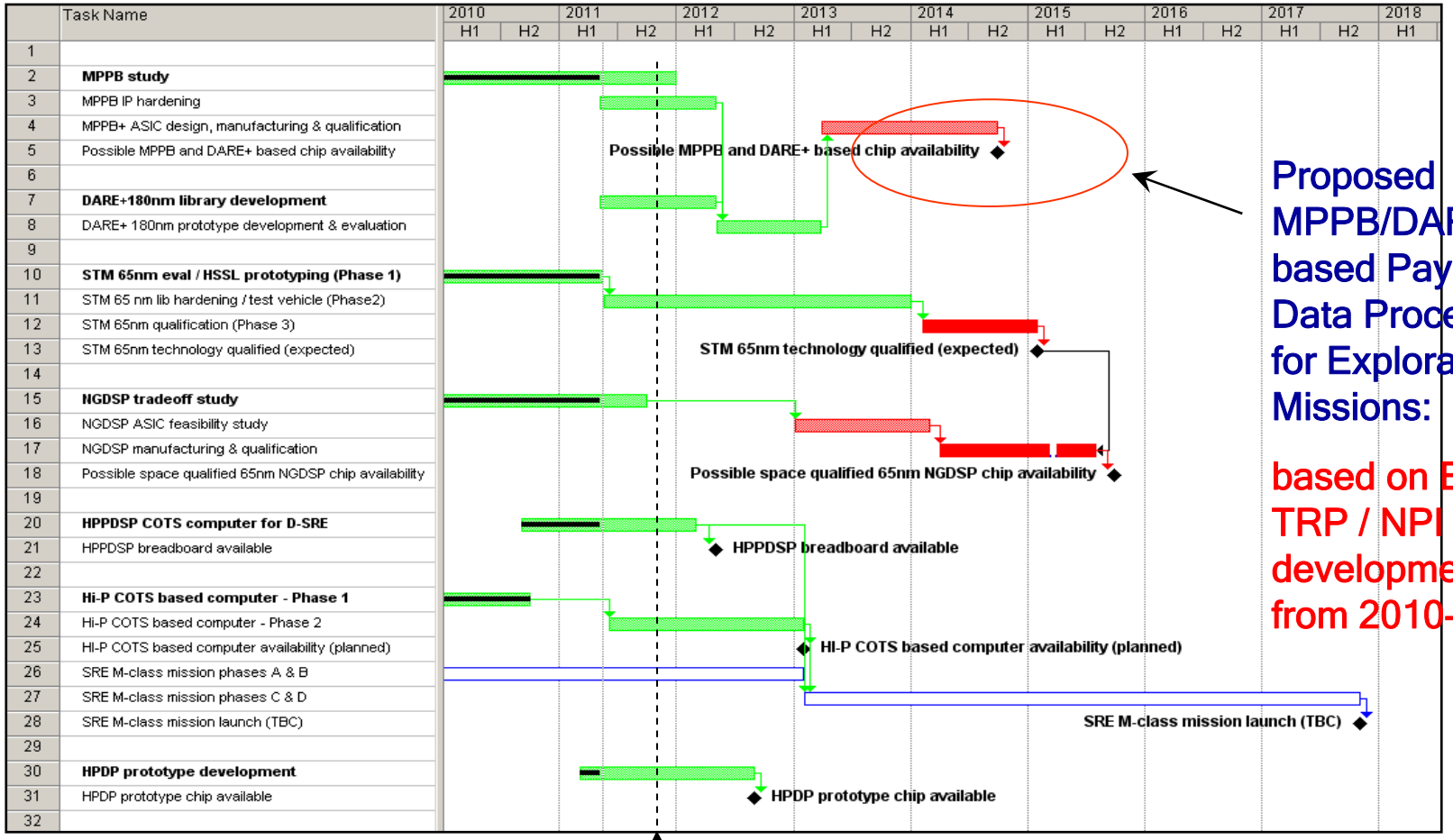
Expected Performance – proposed MPPB based chip vs. LEON2

Benchmark	*Proposed Chip @ 50 MHz*	*LEON2 @ 50 MHz*	*Speedup factor*
1024 pt FFT	~ 66 µsec	~2430 µsec	~37
FIR filter 1 tap	~10 nsec (1 DSP; 2 available)	~166 nsec*	~16/33 (1 DSP / both DSPs)
1 Megapixel image (random 12 bit) Lossless CCSDS compression	few seconds**	~71.7 sec	~3…5 (TBC)**
1 Megapixel image (random 12 bit) Lossy (20 x) CCSDS compression	TBD**	~22.4 sec	TBD**
1 Megasample random data Lossless RICE comp.	TBD** (LEON used)	~3.5 sec	≥1**

- Internal ADC, DAC and multiplexer save power and PCB space
- High radiation hardness (1 Mrad), FDIR options, power saving modes (redundant DSP)
- operation without external RAM possible (SpW RMAP + on-chip memory)

* Extrapolated form similar GPP; ** final benchmark results not available yet

Payload Data Processing Hardware developments: Schedule



Proposed MPPB/DARE180 based Payload Data Processor for Exploration Missions:

based on ESA TRP / NPI developments from 2010-2013

Funding allocated

No funding allocated

No Funding allocated and expensive

November 2011

Presentation Summary (1)

JUICE has demanding requirements for payload data processing
- Efficient, mature software needed
- Sufficiently performant, low power, rad-hard processing hardware needed

Data compression is essential for efficient use of resources
- A range of standardized algorithms is available, evaluation software too
- Compression should be used for both science and housekeeping data

Novel data processing DSP IP and hardware is becoming mature
- MPPB project has developed scalable LEON2/NoC/ fixed-point DSP system
- Multicore system (3 cores; # DSPs scalable from 2 -> more than 10)
- Performant (~450 Mops @ 50 MHz), 1.6 Gbit/sec NoC bandwidth, flexible
- Includes ADC, DAC, multicore, on-chip RAM
- Comprehensive benchmark software including standard payload algorithms

DARE+ activity will create and validate prototype chip
- Xentium® DSP core, NoC, SpW RMAP, UART, memory tile, etc
- Software benchmarks, ADC/DAC interface, radiation performance

Presentation Summary (2)

Payload Data Processor Chip for Exploration Missions is proposed

- Based on MPPB project and DARE+ library development and chip prototyping
- LEON2, NoC, 2 or more fixed-point DSP system
- Performant (1 GOps or more @ > 100 MHz), 3.2 Gbit/sec NoC bandwidth
- Power efficient (fixed point DSP, clock gating, minimized component number)
- Very high integration: ADC, DAC, multiplexer, HK DAQ, multicore, on-chip RAM
- 3-core chip with on-board ADC/ DAC, RAM feasible with 12x12mm die
- Actual architecture, on-chip peripherals to be tailored for JUICE processing needs

Chip is on TEC-ED's roadmap for data processing hardware development

- Based on MPPB, DARE+ TRP activities, and on-going NPI (2010-2013)
- Development is part of ESA TRP proposals for 2013-2015 period:

"Data Processor for Exploration Missions and Small Satellites"

=> Funding of chip development in TRP requested but not guaranteed (competitive)

=> Alternative (partial ?) funding via the project, or D-SRE CTP ? TBC

=> Funding of a part of the development via GSTP ? TBC

Identification of instrument / mission data processing requirements important

- To be collected at this workshop, consolidated lateron
- Chip architecture to be tailored to cover JUICE payload and mission needs

Proposal for requirements consolidation (day #2)

Day #2 of JUICE instrument workshop

16:00-18:00 Splinter session on data processing: collection of information

- Data throughput
- Peak data rates
- Processing Algorithms
- Performance needs
- Compression needs
- Constraints
- AOB

Consolidation of data processing requirements => input to chip architecture definition

Splinter mtg: 2 hours planned, 14 instruments (?) => ca. 8-10 min per instrument (!)

=> Questionnaire for all instruments has been submitted to team leaders, please return asap – will be discussed in splinter meeting.

Proposal for requirements consolidation (day #2)

Day #2 of JUICE instrument workshop

16:00-18:00 Splinter session – proposed sequence (TBC)

16:00 Wide angle camera
16:10 High Res Camera
16:20 Plasma particle package
Ion mass spectrometer
Low energy Neutral detector (P)
16:40 CIRIS compositional IR spectrometer
16:50 ENA imaging (P)
17:00 PRIDE radio interf. & DE
17:10 Subsurface radar
17:20 Magnetometer
17:30 GALA laser altimeter
17:40 Radio Science instrument
17:50 VIRHIS imaging spectrometer
18:00 ORTIS terahertz IR spectrometer
18:10 Sub-milimetre wave instrument
18:20 Dust telescope
18:30 miniaturized plasma analyzer
18:40 thermal plasma sensor
18:50 DSI-echoes

=> Please submit your Questionnaire in time !

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